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High-Efficiency Solar Cells

Physics, Materials, and Devices

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Preface

As a renewable energy source, solar energy can be harvested and will be increasingly important in the inevitable transition from our current level of dependence on fossil fuels. One of the biggest challenges in photovoltaic technology is how to increase the photocurrent conversion efficiency. Since solar cells were developed several decades ago, consistent efforts have been made in exploring variables that influence optimal efficiency. In recent years, research into high-efficiency solar cells has accelerated with the rapid emergence of new materials and devices showing promising performance characteristics. To achieve further increases in the photocurrent conversion efficiency, it is necessary to choose a suitable material, fabricate a device with proper structure, and to understand the physics behind the materials and devices as a basis for developing new approaches to optimize the materials and device characteristics.

This book addresses these issues comprehensively. It covers the physics needed to understand the performance of a high-efficiency solar cell, presents a variety of novel materials that have emerged in recent years, and describes device optimization approaches such as light-trapping structures and surface plasmons. Chapter 1 is a general introduction to many aspects of high-efficiency Si solar cells developed over the last 20 years. Some representative examples of high-efficiency Si solar cells with excellent performance are presented. Chapter 2 describes the dominant mechanism of radiative recombination in c-Si and the dependence of the intensity of the edge luminescence on the intensity of its excitation. Chapter 3 analyzes the balance between generation, recombination, and transport, and its effect on the photocurrent and open circuit voltage of solar cells for overcoming the Shockley-Quiesser limit. Chapters 4 and 5 focus on nanostructures for use in solar cells, including nanowires and quantum wells and dots. High band gap silicon nanocrystal solar cells are discussed in Chap. 6.

In Chap. 7, thiophene-based copolymers synthesized by electropolymerization and used as a hole transport layer in organic photovoltaic cells are presented. Chapter 8 focuses on molecular engineering of efficient dyes for p-type semiconductor sensitization. Chapter 9 describes the production and characterization of Luminescent Solar Concentrator devices based on the dye Lumogen Red

305 dispersed in a matrix (polysiloxane). Chapter 10 introduces the manipulation of energy and electron transfer processes in a light-harvesting assembly in engineered FRET-based solar cells, and efficient near-infrared absorption donor materials for dye-sensitized and organic solar cells. Chlorophyll-derived- , cyclic-Tetrapyrrole-based Purpurins are described in Chap. 11. Chapter 12 highlights the materials, interfaces, and devices of hybrid solar cells. Chapter 13 studies porous TiO_2 nanoparticles applied in PEDOT: PSS photovoltaic devices.

Chapters 14–21 cover device issues of high-efficiency solar cells. Chapter 14 studies the textured microstructures and the photonic nanostructures for light-trapping structures, aiming to suppress the surface reflection. Anti-reflective silicon oxide p-layer for thin-film silicon solar cells is introduced in Chap. 15. Chapters 16 and 17 cover plasmonic silicon solar cells and plasmon-enhanced excitonic solar cells. Finally, Chaps. 18–21 discuss some key aspects of III–V solar cells, including the interfaces (Chap. 18), the anti-reflective coating (Chap. 19), radiation effects (Chap. 20), and the epitaxial lift-off technology used in III–V solar cells (Chap. 21).

The editors would like to express their great appreciation to all of the authors for their excellent chapters. Their enthusiasm and care as seen in every word makes us believe that this book will be an indispensable reference for students, scientists, and engineers in exploring high-efficiency solar cells. We hope it will be seen in retrospect as a milestone volume in this rapidly developing research area. We also thank Mr. Yanpeng Shi for helpful editorial assistance. All of the postgraduate students in our laboratory, especially those working on high-efficiency solar cells, provided much help and a stimulating environment for research. Our appreciation also goes to Springer staff for their support. Finally, the editors acknowledge the support of the National Natural Science Foundation of China under Grant No. 61274066.

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Chapter 1
Status and Progress of High-efficiency Silicon Solar Cells

Shaoqing Xiao and Shuyan Xu

Abstract High-efficiency Si solar cells have attracted more and more attention from researchers, scientists, engineers of photovoltaic (PV) industry for the past few decades. Many high-quality researchers and engineers in both academia and industry seek solutions to improve the cell efficiency and reduce the cost. This desire has stimulated a growing number of major research and research infrastructure programmes, and a rapidly increasing number of publications in this filed. This chapter reviews materials, devices and physics of high-efficiency Si solar cells developed over the last 20 years. In this chapter there is a fair number of topics, not only from the material viewpoint, introducing various materials that are required for high-efficiency Si solar cells, such as base materials (FZ-Si, CZ-Si, MCZ-Si and multi-Si), emitter materials (diffused emitter and deposited emitter), passivation materials (Al-back surface field, high–low junction, SiO_2, SiO_x, SiN_x, Al_2O_3 and a-Si:H), and other functional materials (antireflective layer, TCO and metal electrode), but also from the device and physics point of view, elaborating on physics, cell concept, development and status of all kinds of high-efficiency Si solar cells, such as passivated emitter and rear contact (PERC), passivated emitter and rear locally diffused (PERL), passivated emitter and rear totally diffused (PERT), Pluto, interdigitated back-contacted (IBC), emitter-wrap-through (EWT), metallization-wrap-through (MWT), Heterojunction with intrinsic thin-layer (HIT) and so

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on. Some representative examples of high-efficiency Si solar cell materials and devices with excellent performance and competitive advantages are presented.

1 Introduction

Among various kinds of renewable energies that have been developed, solar power can be said to be the champion of clean energy since there is no other one being as abundant as our sun. The amount of solar energy reaching our earth within 1 h equals to the total annual energy need of all of mankind, taking into account both heat and electricity. In contrast to fossil fuels, solar energy is starting to be used as the panacea for solving climate change or global warming problems since solar energy sources can provide electricity without giving rise to carbon dioxide and other greenhouse gas emissions. Moreover, it is expected that energy resources on Earth will be almost exhausted and solar energy will have to serve as the main energy source for humans in the next century and beyond.

Silicon-based solar cell invented in 1954 [1], as an important means of the universe space development and competition between American and Soviet in 1960s, has gone through its childhood regardless of the cost. In the 1990s, Si-based solar cell has been industrially commercialized in large scale and the installation of solar cells in personal housing or public facilities has been boosted significantly. For the latest 10 years, Si-based solar cell has reached its mature period because the photovoltaic (PV) market (Si-based solar cell covers 90 % of the PV market) is growing rapidly at an annual rate of 35–40 %, with PV installation around 25 GW in 2012 [2]. A cross-sectional scheme of a typical Si-based solar cell (namely, industrial standard screen-printed p-type Si solar cell) is shown in Fig. 1.1. In general, the light is absorbed in a region more or less close to the surface due to the absorption properties of the material. When incident light is absorbed, electron hole pairs are generated and if their recombination is prevented they can reach the junction where they are separated by the built-in electric field. Even for weakly

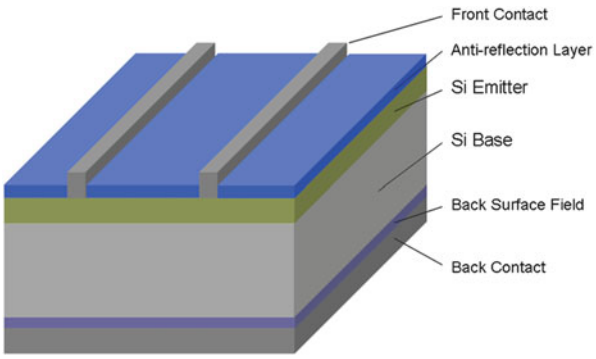


Fig. 1.1 A cross-sectional scheme of a typical Si-based solar cell

absorbing semiconductors like silicon most carriers are generated near the surface. This leads to the typical solar cell structure of Fig. 1.1: the p–n junction separating the emitter and base layer is very close to the surface in order to have a high collection probability for free carriers. The thin emitter layer above the junction has a relatively high conductance which requires a well designed contact grid also shown in the figure. The physics mechanism have been described in many publications [3, 4], and will not be addressed further here.

In the past decade, the cost of Si-based solar cell has been reduced greatly due to the fact that the conversion efficiency increases drastically with the introduction and application of more sophisticated technologies. However, the production cost of Si-based solar cell is still high when compared with conventional fossil-fuel based technologies. Therefore, a large number of research groups all over the world have been devoting to high-efficiency technologies and low-cost technologies. Low-cost technologies are often related to the cost reduction of original material (Si) production, manufacturing facilities, energy consumption and manpower. They are out of scope of this chapter and are not discussed. High-efficiency technologies usually involves novel design of solar cell devices, optimization of light absorption, effective collection of photo-generated carriers, suppression of recombination loss of photo-generated carriers, reduction of electrode area and so on. These technologies result in a variety of high-efficiency Si-base solar cell devices, such as passivated emitter and rear cell (PERC) devices, passivated emitter and rear locally diffused (PERL) cells, passivated emitter and rear totally diffused (PERT) cells, Pluto-cells, interdigitated back-contacted (IBC) solar cells, emitter-wrap-through (EWT) solar cells, metallization-wrap-through (MWT) solar cells and Heterojunction with intrinsic thin-layer (HIT) solar cells.

A high-efficiency silicon-based solar cell not only requires a high-quality p–n junction, whether which is a homojunction or heterojunction, but also requires other functional materials that can enhance the light absorption, provide front and back surface passivation, provide back-surface-field (BSF), act as electrodes to collect currents and so on. For high-efficiency Si-based solar cells, the base material refers to silicon wafer including mono-crystalline (mono-Si) and multi-crystalline (multi-Si) silicon, while the emitter material can be the same kind as the base material for homojunction or amorphous silicon (a-Si) for heterojunction. The functional materials used in high-efficiency silicon-based solar cells usually include silicon nitride (SiN_x), silicon oxide (SiO_2 and SiO_x), aluminium oxide (Al_2O_3), hydrogenated amorphous silicon (a-Si:H), aluminium–silicon alloy, zinc oxide (ZnO), indium tin oxide (ITO), aluminium (Al), silver (Ag), titanium (Ti), etc. These materials have been extensively studied and reported anywhere, from journal literatures to proceeding of symposium.

We feel pleased to write this chapter since high-efficiency Si solar cells substantially step a bright new field with superior importance. The main objective of this work is to create a platform for knowledge sharing and dissemination on latest advances in the areas of high-efficiency solar cells and to provide a comprehensive overview of recent achievements. In this chapter, we explain the most important properties of every material that serve as indispensible part of Si-based solar cell to

contribute to high efficiency, and shed a light on some of the most important points and subjects raised in individual contributions, and also give a brief survey of relevant research efforts in a broader context. The device design and physics mechanism of all kinds of high-efficiency Si solar cells are carefully discussed. In addition, the most significant milestones achieved in each high efficiency Si-based solar cell device are pinpointed and the corresponding opportunities and challenges for large-scale commercialization are also identified. Finally, the long list of relevant references will save time and effort for those producing literature surveys for whatever purpose.

This chapter is organized as follows. Since Si wafer is the core of high-efficiency Si-based solar cells, we first introduce Si material including mono-Si and multi-Si. In this section, the growth mechanisms and characteristics of CZochralski silicon (CZ-Si), float-zone silicon (FZ-Si), magnetically grown CZochralski silicon (MCZ-Si) and multi-Si materials are elaborated. Then we briefly discuss the emitter materials including diffused emitter and deposited emitter. The former induces a homojunction, while the latter usually creates an amorphous–crystalline heterojunction. Next, we present the development and status of most common passivation materials, such as back surface field (BSF) including aluminium–silicon alloy and $p–p^+$ or $n–n^+$ high–low junction, silicon oxide (thermally grown SiO_2 and deposited SiO_x), silicon nitride (SiN_x), aluminium oxide (Al_2O_3) and hydrogenated amorphous silicon (a-Si:H), due to extensive and profound researches in this area. The growth method, passivation performance, processing parameters and their relations of every passivation material are systematically discussed. Also, whether the chemical passivation or field-effect passivation is dominant (or coefficient) in every material is pinpointed. Fourth, other functional materials including antireflective materials, transparent conductive materials and metal electrode materials are briefly presented. In the fifth section, the development and status of a variety of high-efficiency solar cell devices such as PERC, PERL, PERT, Pluto-PERC, Pluto-PERL, IBC, EWT, MWT and HIT are carefully reviewed. The design concept, unique feature and competitive advantage of every high-efficiency Si solar cell device are highlighted. The cell efficiency evolution of every high-efficiency Si solar cell device is also briefly reviewed. This chapter ends with a short summary in the last section.

2 Materials

2.1 Base Material: Mono-Si and Multi-Si

Silicon-based solar cell technology benefits greatly from the high standard of silicon technology developed originally for transistors and later for semiconductor industry. This applies as well to the quality and availability of single crystal silicon of high perfection. In semiconductor industry, more than 85 % of monocrystalline Si (mono-Si) material is grown based on Czochralski (Cz) method [5–7]. Therefore,

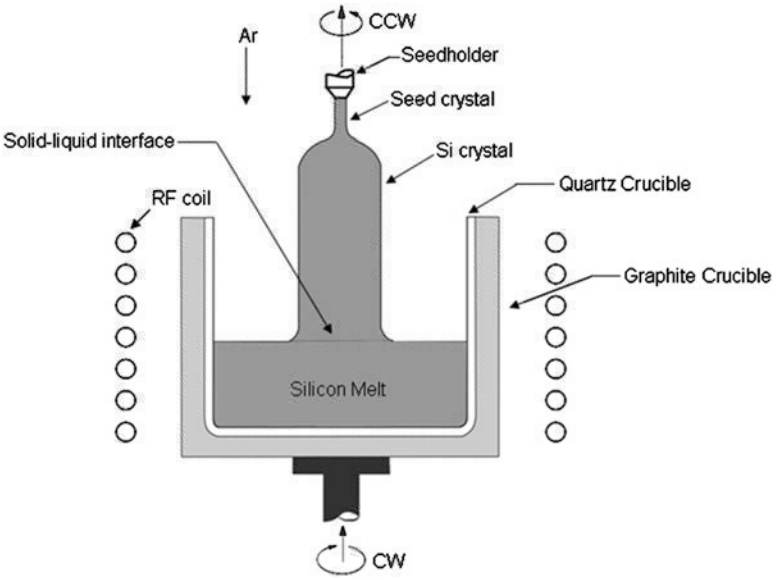


Fig. 1.2 A scheme of Czochralski method for mono-Si growth (*CW* clock-wise, *CCW* counter clock-wise)

in the first years only Cz grown mono-Si were used for solar cells. The growth principle of this method is shown in Fig. 1.2. Polycrystalline Si material in the form of fragments is placed in a quartz crucible located in a graphite crucible and melted under inert gases by induction heating [8]. A seed crystal with a certain orientation (like <111>) placed in seedholder is immersed into the melted liquid. Although the seed crystal will be partially melted, the tip of other unmelted part will contact the melt surface. Then as the seed crystal is slowly withdrawn under rotation, a huge single crystal will be formed at the solid–liquid interface as a result of gradual cooling. A standard growth velocity of Cz-grown mono-Si is several millimetres per minute. The silicon melt reacts with every material to a large extent. Only silica can be used as a crucible material, because its product of reaction, i.e. silicon monoxide, evaporates easily from the melt. Even so, approximately 1 % of the oxygen from the crucible goes into the mono-Si ingot [9, 10] and thus Cz grown mono-Si materials contain 10^{17}–10^{18} cm^3 of mainly interstitial oxygen. Mono-Si material grown by Cz method is free of dislocation but still contains point defects. The type of point defect and their concentration are controlled by (1) the V/G ratio, where V is the growth rate and G is the temperature gradient; (2) the cooling rate, $V \times G$; and (3) the oxygen level [11].

An alternative crystal growth technique is the float zone technique (Fig. 1.3), which can grow Si crystals with lower impurities (mainly interstitial oxygen) than that prepared by Czochralski method. A rod of solid and highly purified but polycrystalline silicon with a seed crystal at the bottom is kept in perpendicular

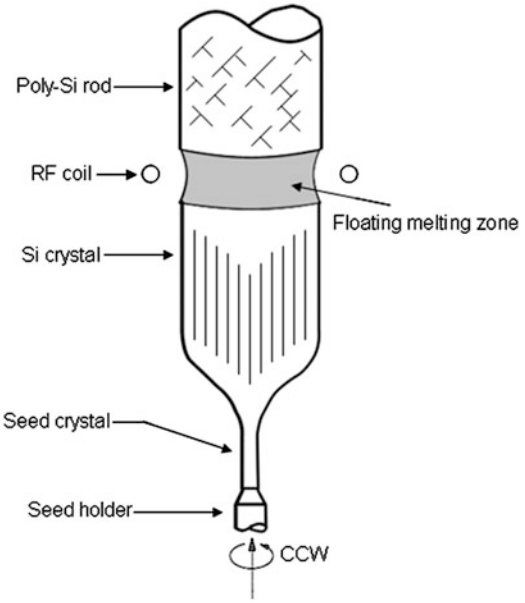


Fig. 1.3 Principle of the float zone (Fz) technique for mono-Si growth (*CCW* counter clock-wise)

direction and rotated. This rod is sealed in a quartz pipe filled with inert gas (Ar). During the growing process, a small area of the polycrystalline silicon rod is melted by induction heating using rf coil. The rf heater sweeps over the entire polycrystalline silicon rod from the bottom seed crystal to the upper, thus the floating molten zone sweeps as well over the entire polycrystalline silicon rod. The silicon melt is supported by the surface tension between the melting silicon and the growing solid silicon. As the floating melting zone moves up, a highly purified single crystal is formed at the recrystallization zone according to the extended direction of seed crystal. This material is of exceptional purity because no crucible is needed but is more costly than Cz material. In particular, it has a very low oxygen contamination which cannot be avoided with the Cz-material because of the quartz crucible. Float zone (Fz) Si material is frequently used in lab research work and record efficiency for Si solar cells has often been manufactured with Fz Si material. However, it is too expensive for regular solar cell production, where cost is of overriding importance.

Recently, interesting results have been obtained with an advanced technique, magnetically grown Czochralski (Mcz) silicon by Shin-Etsu Handotai in Japan. The principle has been described earlier in [12]. The magnetic field interacts with the free electrons of the silicon and retards convective melt flows. The transport of oxygen from the crucible walls is minimized. Furthermore the distribution of impurities is more uniform.

For solar cells, as well as for all other devices the crystal rods are separated into wafers of 0.2–0.5 mm thickness by multiwire sawing. A wire of several kilometres in length is moved across the crystal in an abrasive suspension, whilst being wound

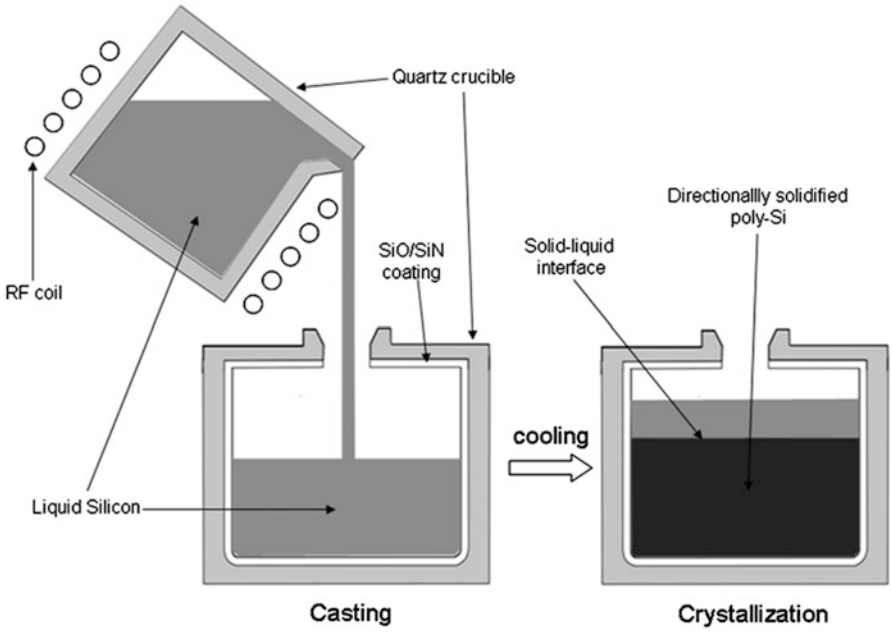


Fig. 1.4 A scheme of block casting for poly-Si

from one coil to another. In this manner, thinner wafers can be produced and sawing losses are reduced by about 30 %.

Since the cost of silicon material is the highest proportion of the cost of a silicon-based solar cell, great efforts have been made to reduce these costs. The dominant technology is block casting [13] which avoids the costly pulling process in comparison with Cz method. Silicon is melted in a square quartz crucible and then poured into a square SiO/SiN-coated quartz crucible (Fig. 1.4). The SiO/SiN coating is used to prevent poly-Si ingot from breaking during the cooling and crystal growth processes since the thermal expansivity of Si is so much larger than quartz that a buffer layer (SiO/SiN coating) is needed. Controlled cooling produces a polycrystalline silicon (poly-Si, also called multicrystalline silicon: multi-Si) block with a large crystal grain structure [14]. The grain size is some millimetre to centimetre and the silicon blocks are also sawn into wafers by multiwire sawing. Poly-Si is only used for solar cells and not for other semiconductor devices. The crystal structure of poly-Si ingot obtained by casting based on a unidirectional growth technique is markedly different from that of mono-Si, as illustrated by the formation of grain boundaries and the distribution of crystallographic orientations, which prevent the realization of high-efficiency solar cells. However, it is much cheaper than mono-Si material. Another advantage of poly-Si is that the blocks can be manufactured easily into square solar cells in contrast to pulled mono-Si rods which are always round. It is much easier to assemble poly-Si wafers into modules with

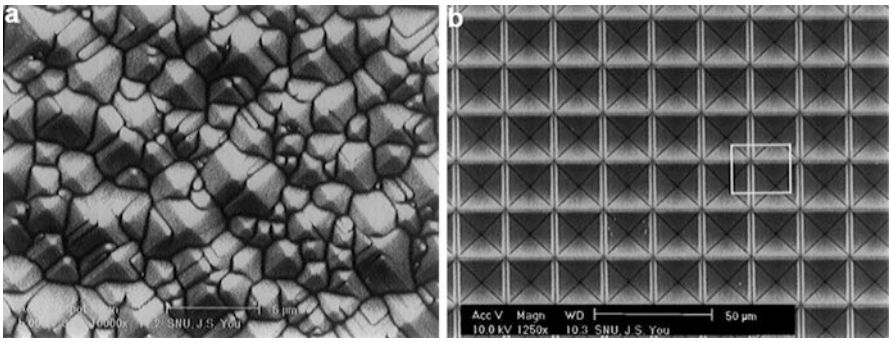


Fig. 1.5 SEM images of mono-Si surface showing random distributed pyramids (**a**) and uniform inverted pyramids (**b**) (reproducible from [29])

nearly complete utilization of the module area. Thus, the lower efficiency of poly-Si material tends to disappear at the module level.

In the present-day PV market, mono-Si (Cz) and poly-Si solar cells cover almost 90 % of the total solar cell production, with an average efficiency of 18.5 % and 16.5 %, respectively. Due to the advantages of poly-Si as described above, the proportion of poly-Si solar cells is increasing year by year [15]. In order to obtain high-quality poly-Si material, various new methods such as dendritic casting [16–18], seeded casting [19–21] and other methods [22–24] have been presented by controlling macro- and microstructures of poly-Si ingots in recent years. The crystal growth phenomena during melt growth processes including the morphological transformation of crystal–melt interfaces, grain boundary formation, parallel-twin formation and faceted dendrite growth have also been carefully studied [25]. These contexts are out of scope of this chapter and will not be discussed (please see Refs. [15–25] if the readers are interested) since high-efficiency Si-based solar cells are always fabricated based on mono-Si material (including Cz, Fz and MCz Si material). Advanced solar cells with high efficiency require single crystals of very high perfection other than poly-Si with various types of defect, such as grain boundaries, dislocations, sub-grain boundaries and metallic impurities.

For fabricating high-efficiency Si-based solar cells, an indispensable step after the preparation of silicon wafers is surface texturization. As the refractive index of Si is very high, reflection at the surface of solar cells has to be minimized. Surface texturing not only reduces reflection but also provides oblique coupling of light into the cell. In this manner, the radiation paths are increased and the absorption of infrared radiation is therefore enhanced. Wet chemical treatment is still state of the art to texturize the surface of mono-Si. In general, randomly distributed pyramids (see Fig. 1.5a) are obtained on the surface of mono-Si (100) by a standard anisotropic etching treatment in alkaline solution [26–29]. By using an etching mask (pattern), the pyramids are etched down into the silicon surface rather than etched pointing upwards from the surface, so uniform inverted pyramids (see Fig. 1.5b)

can be produced on the surface [29]. Such texturing is not suitable to apply on poly-Si substrate due to its anisotropic nature. Presently, technique such as acid etch [30, 31] and reactive ion etching [32, 33] have been developed to texturize the surface of poly-Si. Acid texturing, performed with solutions containing hydrofluoric acid (HF) and nitric acid (HNO_3) that tend to isotropically etch poly-Si, can result in features with rounded (pit) surfaces, as opposed to flat-sided features which arise from alkaline etches.

2.2 Emitter Materials

2.2.1 Diffused Emitter

The emitter layer is a requisite to form the p–n junction for (high-efficiency) Si-based solar cells. Nowadays, most Si solar cell manufacturing companies in the world use p-type silicon wafer as the base material. Therefore, phosphorus precursors such as gaseous $POCl_3$, solid paste P_2O_5 are utilized to realize the phosphorus diffusion and thus the n-type doping [34]. The n-type base is only used in lab for high-efficiency Si-based solar cell. In order to fabricate a p–n junction on the n-type Si wafers, gaseous BBr_3 is employed as the precursor to realize the boron diffusion. Here, we just briefly describe the diffusion process of phosphorus, which is the mainstream in industrial process for Si-based solar cells [35–37]. The diffusion process mainly consists of two processes: i.e. pre-deposition and drive-in. The Si wafers in quartz boat are loaded into the furnace and then heated to 800–900 °C. Nitrogen is bubbled through the temperature-controlled $POCl_3$ liquid source to deliver dopant in vapour form to the furnace. $POCl_3$ vapour is mixed with oxygen and then leaded into the furnace and reacts with the Si surface in high temperature. This pre-deposition process creates a thin and solid doping silicon oxide layer (P_2O_5-SiO_2) with high concentration on the Si surface. The chemical reactions are shown below:

$$4POCl_3 + 3O_2 \rightarrow 2P_2O_5 + 6Cl_2 \tag{1.1}$$

$$2P_2O_5 + 5Si \rightarrow 4P + 5SiO_2 \tag{1.2}$$

Then these wafers are heated to 850–950 °C for drive-in process by simultaneously stopping supplies of dopant source. At such high temperature, the phosphorus in the silicon oxide layer can diffuse rapidly into Si wafer. Consequently, the emitter profile depends on the processing temperature and time. During the diffusion process, the phosphorous silicate glass (PSG) can also be formed through the reaction between O_2, $POCl_3$ and Si. The PSG layer (20–40 nm) is usually removed by acid etch in industry.

2.2.2 Deposited Emitter: p–(n-) a-Si:H

Apart from the above diffusion process for the formation of an emitter layer, there is another deposition process that can also fabricate a p–n junction on Si surface. Thin films of p-type (or n-type) hydrogenated amorphous silicon (a-Si:H) are usually deposited on n-type (or p-type) Si surface to fabricate a p–n junction. These thin films are commonly synthesized using SiH_4, H_2 and B_2H_6 (or PH_3) precursors by a variety of deposition methods, such as plasma enhanced chemical vapour deposition (PECVD) [38–42], hot-wire chemical vapour deposition (HWCVD) [43–45] and inductively coupled plasma chemical vapour deposition (ICPCVD) [46, 47]. Different from the diffusion process where a homojunction is produced (both base and emitter are mono-Si or poly-Si materials), the deposition process typically creates a heterojunction since the base is crystalline while the emitter is amorphous. Amorphous–crystalline silicon heterojunction solar cells have attracted increased attention since it was demonstrated that high efficiencies (21 %) can be achieved on Cz silicon using a simple structure and only low temperature processes [48].

Such emitter is formed by a low temperature deposition process and not by the conventional high-temperature diffusion process above 900 °C. The deposition process has the advantage of not only being a low temperature process, but is also a process in which the doping, band gap, and thickness of the deposited layers can be controlled and profiled accurately, which offers new opportunities for optimizing the device performance. Because of the low temperature process, cheaper lower-quality Si substrates (which would normally degrade in a high-temperature process) can be used. Back surface fields (BSFs) and passivating layers can also be made by deposition and the details will be discussed in the flowing context.

2.3 Passivation Materials

Since the PV solar cells generate solar power by converting the incident illumination into electron-hole pairs and separating the electron-hole pairs to flow out, high-efficiency Si solar cells can be obtained only when both the loss of photo-generated carriers and the loss of sunlight entering into solar cells are reduced [49]. In other words, to produce high-efficiency Si solar cells, the effective minority carrier lifetime (τ_{eff}) should be lengthened and the surface-reflection loss of sunlight should be reduced. To enhance the effective minority carrier lifetime, the surface recombination of photo-generated carriers has to be minimized by using a passivation layer (A reduction in surface recombination is called surface passivation). To reduce the optical loss due to the reflection at the air–c-Si interface, the use of an anti-reflective layer is preferred. We first discuss the surface passivation scheme for high-efficiency Si-based solar cells because the minimization of electronic losses at

the crystal silicon surface is a more delicate challenge compared with the optical management by conventional methods like using an antireflection layer.

Physically, the surface passivation is achieved by two effects: the direct saturation of defects (also called chemical passivation) and the field effect passivation. The chemical passivation aims to reduce the surface defects by saturating the remaining silicon dangling bonds. Technologically, this strategy is much more sensitive to the presence of defects at the surface than the field effect passivation and usually related to a passivating layer deposited or grown over the c-Si surface. In this sense, the cleaning steps before deposition or growth of the passivating film are of paramount importance to reduce the surface defect density. In the last step of RCA [50] or other chemical cleaning methods the wafer is dipped into diluted HF solution in order to eliminate the native oxide at the c-Si surface. Furthermore, this immersion may also achieve a perfect coverage of the c-Si surface dangling bonds by atomic hydrogen (leading to very low surface recombination velocity values [51]). Other approaches to wafer cleaning that are economically less expensive than RCA and therefore easier to transfer to solar cell mass production are dry cleaning methods. They normally consist of subjecting the wafer to plasma with an etching gas [52–54]. The method is also helpful to roughen the surface, thus providing a light trapping scheme. Last but not the least, some passivation techniques are based on dangling bond saturation by atomic hydrogen. For instance, it is common to add molecular hydrogen (H_2) into the precursor gases when a passivating layer of amorphous hydrogenated silicon-based compound like a-Si:H, amorphous hydrogenated silicon nitride (a-SiN_x), amorphous hydrogenated silicon carbide (a-SiC_x:H), amorphous hydrogenated silicon oxide (a-SiO_x:H) is deposited [55]. The same idea is exploited in annealing the samples within a N_2/H_2 atmosphere (Forming Gas).

The field effect passivation consists of producing a band bending at the silicon surface, thus creating an electric field. This electric field will make one type of carriers hard to reach the surface defect centre. Therefore, the recombination rate is strongly reduced since two types of carriers, namely, electrons and holes, are needed to complete the recombination process at the surface defect centre. Technically, the electric field can be produced in several ways, by depositing a charged film or by creating a heavily doped region. Dielectric films storing a high charge density, like amorphous silicon nitride (SiN_x), have already been successfully applied in solar cell industry for both mono- and poly-crystalline silicon solar cells. Recently, another dielectric film, namely, Al_2O_3 with a high negative fixed charge density, which is different from the positive fixed charge density of SiN_x, has attracted much attention as a passivation scheme for high-efficiency Si solar cells. It may also be possible to deposit or grow dielectric layers with a relatively low charge density, like thermally silicon dioxide (SiO_2), and apply an external voltage or an electrostatic charge at the surface by a corona charging instrument to provide the field effect. In the case of heavily doped regions, they can be either high–low junctions with the same type of impurities (p^+–p or n^+–n) or p–n junction with opposite doping types. The p^+–p combination is commonly employed at rear side of industrial p-type silicon solar cells using silicon–aluminium alloy and aluminium,

contacting the base and achieving at the same time what is called as back surface field (BSF). On the contrary, the p–n junctions consisting of Si base and emitter are usually contacted and located at the front side of the solar cell, though they can also be not contacted (in the case they are called floating junctions).

In principle, most dielectric layers such as SiN_x, Al_2O_3 and SiO_x provide not only chemical passivation but also field effect passivation. However, a-Si:H can only provide chemical passivation, which is mainly used for high-efficiency silicon heterojunction solar cells. The ability of a passivation layer to perform c-Si surface passivation can be evaluated by the effective minority carrier lifetime (τ_{eff}) of the double-sided passivated c-Si wafer. The effective minority carrier lifetime is currently measured by using the quasi-steady state photoconductance decay (QSSPCD) technique, which was invented by Sinton and Cuevas in 1996 [56]. The effective surface recombination velocity S_{eff} is correlated with the effective minority carrier lifetime τ_{eff} through the following equation:

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{bulk}}} + \frac{2S_{\text{eff}}}{d} \tag{1.3}$$

Where τ_{bulk} is the bulk lifetime of silicon and d is the substrate's thickness. By neglecting the bulk lifetime ($\tau_{\text{bulk}} \rightarrow \infty$), we can obtain the upper limit of S_{eff}.

2.3.1 Back Surface Field (BSF)

Back surface field (BSF) consists of creating a high–low junction, i.e. $p–p^+$ or $n–n^+$ at the rear side of the solar cell (depending on the doping type of the substrate) that builds a field effect passivation. For industrial standard screen-printed p-type Si solar cells, the state-of-the-art rear side passivation is realized by the $p–p^+$ junction using aluminium BSF. Aluminium paste is a standard electrode material for the rear side contacting. Aluminium–silicon alloy can be produced after a firing at a relatively low temperature of 577 °C (the eutectic temperature), with aluminium acting as a p^+ accepter. This property is used to create an already contacted $p–p^+$ high–low junction. The aluminium BSF is optimal for industrial solar cells since it provides good contact, field effect passivation and reflection at the rear side in a very simple step. However, the maximum open circuit voltage provided by this structure is around 630 mV (corresponding to rear surface recombination velocities ranging from 200 to 600 cm/s [57, 58]), which is insufficient for high-efficiency Si solar cells. For high-efficiency Si solar cells, the Al BSF is partially used such as the implementation of a passivated rear with local Al BSF (PERC-type solar cell).

For high-efficiency HIT solar cells, the rear side passivation is controlled by both the chemical passivation of intrinsic a-Si:H films and the field-effect passivation of the high–low junction, i.e. $p–p^+$ or $n–n^+$. Thin films of intrinsic and p^+ (or n^+) a-Si:H are deposited on the rear side of p-type (or n-type) Si wafers to induce these passivation effects. The chemical passivation of intrinsic a-Si:H films will be discussed in Sect. 2.3.5.

2.3.2 SiO_2 and SiO_x

Thermally grown silicon dioxide (SiO_2) is one of the pioneer passivation schemes for high-efficiency silicon-based solar cells due to the high-quality interface between SiO_2 and c-Si. The formation of SiO_2 is often accomplished by exposing the Si substrate to an oxidizing environment at elevated temperature. Thermal oxidation can be carried out in tube furnaces or in rapid thermal anneal furnaces in O_2 ($T \sim 950$–$1{,}000$ °C) or H_2O-vapour ($T \sim 850$–900 °C) atmosphere [59–61]. The corresponding chemical reactions involved are expressed by:

$$Si + O_2 \rightarrow SiO_2 \tag{1.4}$$

$$Si + 2H_2O \rightarrow SiO_2 + H_2 \tag{1.5}$$

According to the model predicted by Deal and Grove [62] the thickness of SiO_2 depends on the root square of the processing time, the process temperature, the orientation of crystalline surface, and the atmosphere type. In dry atmosphere the growing rates are very low. For instance, to grow a 110 nm thick layer (adequate for antireflective layers on Si) the wafer needs to undergo dry thermal oxidation for 70 min at 1,100 °C. With the H_2O molecule being smaller than the O_2 molecule its diffusion through the already existing oxide layer to the Si–SiO_2 interface is much faster [63] and consequently the growing rate is significantly higher in wet atmosphere [64–66]. However, the quality of the Si–SiO_2 interface is poorer than that obtained by dry oxidation. Therefore, in order to achieve thick SiO_2 layers with good interface quality in a reasonable time it is common to combine dry and wet thermal oxidation.

From the viewpoint of surface passivation, silicon dioxide works mainly by reducing the density of states at the interface. Analysis of the charge density reveals that there is a positive fixed charge density (Q_f) within the dielectric layer with a value in the range of 10^{10}–10^{11} cm^{-2} [67, 68]. However, this value level is not high enough to activate the field-effect passivation, which is usually accompanied by a fixed charge density of $>10^{12}$ cm^{-2} [69]. Hence, an important benefit of thermal SiO_2 is the high level of chemical passivation that can be achieved for both n- and p-type Si surfaces over a wide range of relevant doping levels.

To further improve passivation effect, forming gas anneal treatment and Al-anneal treatment [60, 61, 70–72] are often used after oxidation. The former is achieved by exposing the passivated wafer to the forming gas at 400 °C for a certain time. The latter is realized by evaporating a sacrificial aluminium layer over the SiO_2 followed by an annealing at 400 °C in H_2O atmosphere. During this anneal, atomic hydrogen is created from the oxidation of the aluminium by H_2O. For both processes, the hydrogen that is introduced during the annealing process diffuses easily towards the interface and saturates most of the remaining dangling bonds, thus leading to a reduction of the interface state density [70, 73].

Up to now, the best results of thermally grown SiO_2 surface passivation after forming gas annealing or Al-annealing allow S_{eff} values below 3 cm/s for both n- and p-type Fz c-Si wafers with a representative resistivity of 1–10 Ω cm [72].

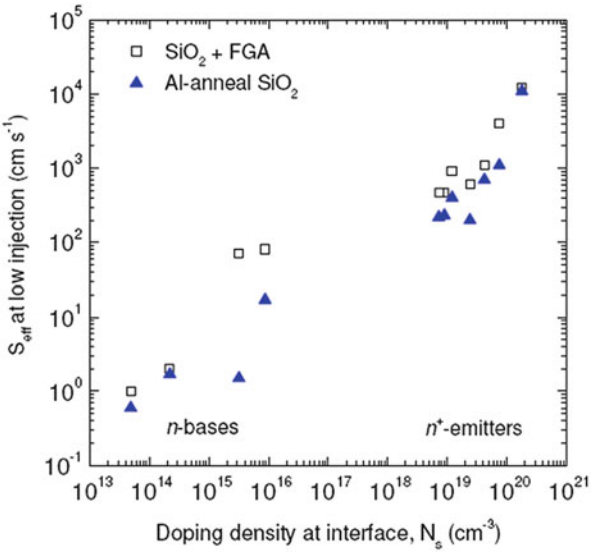


Fig. 1.6 Surface recombination velocity of phosphorus doped bases and emitters as a function of the doping density at the interface provided by thermally grown silicon dioxide. (Reproducible from [77])

For Cz c-Si wafers with high resistivity (>100 Ω cm), the lowest S_{eff} values is below 10 cm/s [74, 75]. For lower resistive Cz c-Si wafers this excellent surface passivation is still providing very good results (on p-type silicon $S_{\text{eff}} < 20$ cm/s for 14 Ω cm [68] and $S_{\text{eff}} = 41$ cm/s for 0.7 Ω cm [76] are achieved). The surface recombination velocity of n-type bases and emitter as a function of the doping density at the interface for silicon dioxide with FGA and Al-anneal treatments is shown in Fig. 1.6 [77]. The trend shown in Fig. 1.6 is actually a general trend for all surface passivation strategies, i.e. the surface recombination velocity increases with doping density due to a higher presence of defects introduced at the interface.

Owing to the excellent passivation properties in combination with good optical properties provided by thermally grown SiO_2, many research groups have devoted to high-efficiency Si solar cell devices using thermally grown SiO_2 and its stack with other functional materials like silicon nitride or aluminium oxide as the passivation and/or antireflection scheme. Particularly, Zhao et al. at the University of New South Wales achieved a world-record efficiency of 24.0 % [78] at a standard test conditions (AM 1.5, 25 °C) with the concept of PERL cell based on Fz Si materials and SiO_2 passivation scheme. With the same concept of cell the efficiency was later improved up to 24.7 % [79], which is the present efficiency record of c-Si solar cells working at 1 sun illumination.

Although thermally grown SiO_2 provides excellent passivation properties and thus is quite suitable for high-efficiency Si solar cells, it cannot yet be applied in conventional Si solar industry since it still suffers from inherent disadvantages such as extremely high process temperature and low deposition rate, which are not desirable from not only the throughput but the process compatibility viewpoint. Therefore, various other methods have been explored for developing SiO_x surface passivation films at low temperatures, such as PECVD [80, 81], ICPCVD [82] and

expanding thermal plasma (ETP) technique [83]. These low-temperature processes can be technologically interesting as they open up the possibility for using materials that are less thermally stable and avoids the risk of bulk lifetime degradation. For ICPCVD developed by our group, the minority carrier lifetime in the SiO_x:H-passivated p-type Cz Si substrate is up to 428 μs and the corresponding surface recombination velocity is as low as 70 cm/s [82]. Hoex et al. [83] also developed SiO_2 films deposited by means of ETP technique at high deposition rates in the range of 0.4–1.4 μm/min using an argon/oxygen/octamethylcyclotetra-siloxane (OMCTS) gas mixture. These plasma-deposited SiO_2 films yield effective surface recombination velocities as low as 54 cm/s on 1.3 Ω cm n-type silicon after a 15 min forming gas anneal at 600 °C. Sai et al. studied the fixed charge density values for different growing conditions [68], measuring low values for dry oxidation ($2–10 \times 10^{10}$ cm^{-2}), higher values for wet oxidation ($2–4 \times 10^{11}$ cm^{-2}), and significantly higher values for CVD ($>10^{12}$ cm^{-2}). However, higher Q_f values are not beneficial to the surface passivation since it has been deduced that the value of the fixed charge density (Q_f) is approximately proportional to the density of states at midgap position ($D_{it,\ midgap}$). On the contrary, surface passivation gets worse as Q_f increases due to the increment of $D_{it,\ midgap}$. This is the reason why the lowest S_{eff} values are always obtained for dry thermal oxidation.

2.3.3 Amorphous Silicon Nitride (SiN_x)

The present state of the art in surface passivation and antireflection of industrial silicon wafer solar cells including mono-Si and poly-Si is amorphous hydrogenated silicon nitride (a-SiN_x:H or SiN_x for brevity) synthesized by PECVD or microwave plasma PECVD [72, 84–88]. SiN_x is usually made from a gas mixture of SiH_4 and NH_3. Silane acts as silicon and hydrogen sources. The ammonia, in addition to being a source of nitrogen, has a tendency to deposit SiN with a high ratio of incorporated hydrogen [89]. In SiH_4/NH_3 discharge, electron collisions with SiH_4 and NH_3 produce H and all of the SiH_n and NH_m: SiH_3, SiH_2, SiH, Si, NH_2, NH, N. The reactions between nitrogen-, silicon- and hydrogen-species in the plasma results in an amorphous solid deposit commonly denoted a-SiN_x:H.

The expansion of this low temperature plasma technology is attributed to a substantial improvement in solar cell efficiency resulting from the deposition of SiN_x in conjunction with fire-through techniques for the metallization step. This enhancement can be ascribed to three driving forces. First, a large amount of hydrogen originating from the plasma gas dissociation and incorporated in the SiN_x film can be driven into the solar cell during the metallization step, leading to an excellent bulk passivation for c-Si or poly-Si solar cells [90, 91]. This effect is particularly significant for poly-Si solar cells [88, 91, 92] since poly-Si contains various types of defects in the bulk as described in Sect. 2.1. The second driving force is the antireflective (ARC) properties of the nitride layer which reduce significantly the light reflection. Indeed, the optical properties of the material can be varied in a wide range by changing the composition. A representative plot

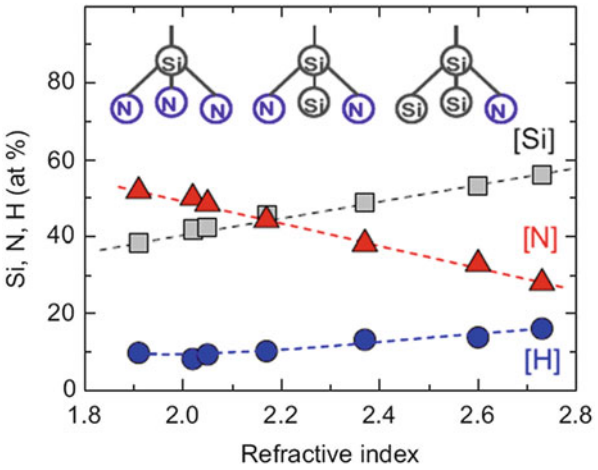


Fig. 1.7 Composition of a-SiN_x:H films in terms of H, Si and N density plotted over the resulting refractive index. The films were deposited in a Roth and Rau MW-PECVD reactor. The atomic densities were obtained by Rutherford backscattering spectroscopy and elastic recoil detection. The *inset* shows some possible bonding configurations of Si (with dangling bonds) where $N_3{\equiv}Si–$ represents the amphoteric K-centre, which is typically positively charged for a-SiN_x:H films on Si substrates (reproducible from [93])

(see Fig. 1.7) presents the material composition in terms of the atomic H, Si and N density as a function of the refractive index [93]. Films with comparatively high nitrogen content (N-rich SiN_x) exhibit refractive indexes of approximately 2, which results in optimal antireflection properties when applied on the front side of a solar cell. In contrast, films with low nitrogen content (Si-rich SiN_x) show higher refractive indexes and therefore higher extinction coefficients, leading to some absorption of light within the film that degrades the antireflection effect. The films also contain a relatively large amount of hydrogen of ~10–15 %, which plays as the first driving force. The third driving force is the surface passivation effect, which is achieved by chemical passivation or/and field-effect passivation.

Whether the chemical passivation or field-effect passivation is dominant in the surface passivation of the a-SiN_x:H films strongly depends on the nitrogen content. When the nitrogen content is relatively low, the Si-rich films exhibit amorphous Si-like properties. In this case, the high level of passivation is mainly governed by chemical passivation. On the other hand, for high nitrogen content, the N-rich films induce a significant amount of filed-effect passivation with fixed positive charge densities of the order of 10^{12} cm^{-2}. This is related to the so-called K-centre (a Si atom backboned with three N atoms) that can be charged positively [see Fig. 1.7 (inset)] [94–97]. In general, Capacitance–Voltage (C–V) measurements of metal-oxide-semiconductor (MIS) structures are used to determine the fixed charge density (Q_f) in the film. A very high fixed charge density $Q_f = 3 \times 10^{12}$ cm^{-2} was measured by Elmiger and Kunst [98] in their SiN_x films prepared by PECVD. In our previous work [99], we also obtained a high fixed charge density of

2×10^{12} cm^{-2} in $SiN_{0.81}$:H films with a refractive index of 2 synthesized by ICP using SiH_4, N_2 and H_2 precursors. Obviously, this field effect passivation is more beneficial for n-type substrates or emitters than p-type Si surfaces due to the positive polarity of charge density at the interface.

In silicon nitride passivation schemes the comparison between chemical passivation and field-effect passivation has been extensively studied. In a recent work [100], the authors systematically investigate the passivation properties of SiN_x:H films prepared by PECVD as a function of the ratio of Si/N. They obtained the best results (n-type Si: $S_{eff} = 4$ cm/s; p-type Si: $S_{eff} = 14$ cm/s) for the Si-rich $SiN_{0.35}$:H films. However, for the N-rich $SiN_{0.78}$:H films the lowest surface recombination velocity (S_{eff}) is 33 cm/s for n-type Si and 68 cm/s for p-type Si, respectively. Note that in the Si-rich films the chemical passivation is dominant while it is contrary in the case of N-rich films. Consequently, it can be deduced that the dominant chemical passivation provides better passivation performances than the dominant field-effect passivation. Nevertheless, the N-rich SiN_x:H films provide an appropriate refractive index around 2 for optimal antireflection and thus are generally adopted as the front passivation and antireflection layer for industrial and high-efficiency Si solar cells. In addition, a firing step is performed after the deposition of silicon nitride in industrial processes as well as in the fabrication processes of some high-efficiency Si solar cells, so it is desirable that the films applied keep or enhance their properties after the firing process. Schmidt et al. [101] showed that films with a refractive index of 2.1 (N-rich SiN_x) enhanced the wafer effective lifetime after a short treatment at 900 °C, while when the index was slightly higher ($n = 2.4$) and therefore the films was a bit more rich in silicon, the tendency was inverted. The reason is closely associated with the denser and thermally more stable properties of N-rich SiN_x:H films in comparison with Si-rich SiN_x:H films. When subjected to a high-temperature treatment, such a layer is believed to induce the release of hydrogen in its atomic form, which consequently leads to an efficient passivation of surface and bulk defects of the Si substrate. This further explains why N-rich SiN_x films with appropriate refractive index of around 2 are generally used in industrial and high-efficiency silicon solar cells.

From the viewpoint of passivation performances, silicon nitride films exhibit a lower level of passivation than silicon dioxide and aluminium oxide. Therefore, N-rich SiN_x films are often incorporated into stacked films such as SiN_x/SiO_2 and SiN_x/Al_2O_3 as a capping layer for high-efficiency Si solar cells due to their dense and thermally stable properties.

2.3.4 Aluminium Oxide (Al_2O_3)

Aluminium oxide (Al_2O_3) has recently emerged as an outstanding passivation scheme for p-type or n-type c-Si wafers or emitters. The field-effect passivation associated with the negative fixed charges near the Al_2O_3–c-Si interface [102–104], proved to be especially beneficial for the passivation of highly doped p-type wafers or emitters. For achieving high-efficiency p-type c-Si wafer solar cells, the conventional Al-back-surface-field (Al-BSF) has to be replaced by a dielectrically

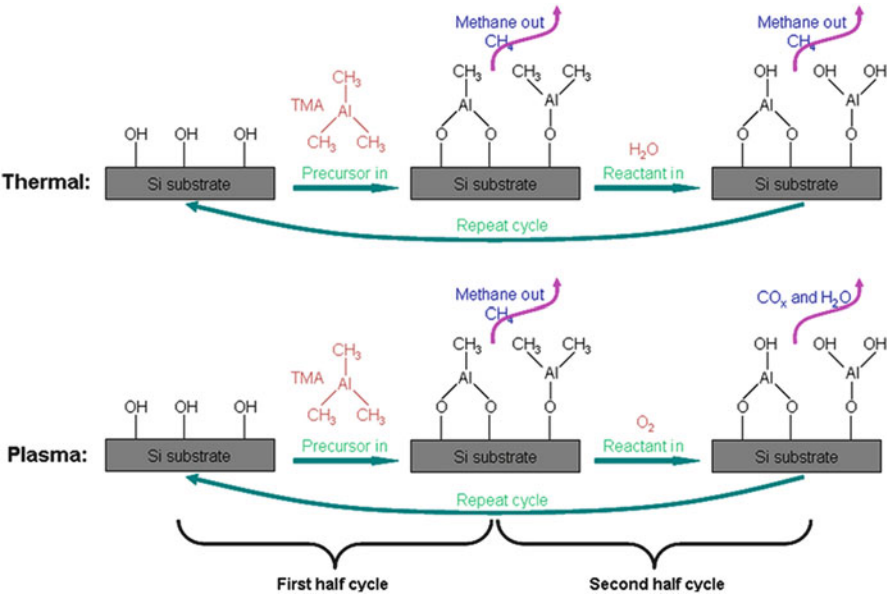


Fig. 1.8 Schematic of one cycle of a thermal and a plasma-assisted ALD process. Each cycle consists of two half-cycles: first, the trimethyl aluminium (TMA) molecules attach to the hydroxyl groups bound to the silicon surface; second, the molecules are oxidized by H_2O (thermal ALD) or an O_2 plasma (plasma ALD)

passivated rear in order to realize better surface passivation and internal reflection as well as reduce wafer bow for thin wafers. Due to the positive polarity of charge density at the SiN_x–Si interface, a-SiN_x:H is not a suitable candidate for the p-type Si rear. As described in Sect. 2.3.1, thermally grown SiO_2 can provide an excellent level of passivation for both p- and n-type Si wafers, and thus has been utilized as the rear passivation scheme for high-efficiency Si wafer solar cells [78, 79]. However, the cost, complexity and a possible adverse impact of high temperatures on the bulk quality make it not appropriate as a first choice. This is why the studies of Al_2O_3 as a passivation scheme for high-efficiency silicon solar cells are becoming a hot and active research area in recent years. Moreover, for high-efficiency n-type Si solar cells a suitable passivation solution of the p^+ emitter is required. The negative charges of Al_2O_3 are an ideal match for the passivation of such emitters in comparison with SiN_x and thermally grown SiO_2. To date, the application of Al_2O_3 on p^+ emitter and on the p-type Si rear has resulted in enhanced solar cell efficiencies up to 23.9 % [105, 106].

In general, Al_2O_3 films with an outstanding surface passivation quality are usually deposited by plasma-assisted as well as thermal atomic layer deposition (ALD) in lab with a very low deposition rate of <2 nm/min [107–110]. In the plasma (or thermal) ALD process, one monolayer of Al_2O_3 is grown per cycle, with each cycle consisting of two half-cycles, as depicted in Fig. 1.8. In the first half-cycle, the trimethyl aluminium (TMA) molecules react with hydroxyl (OH) groups

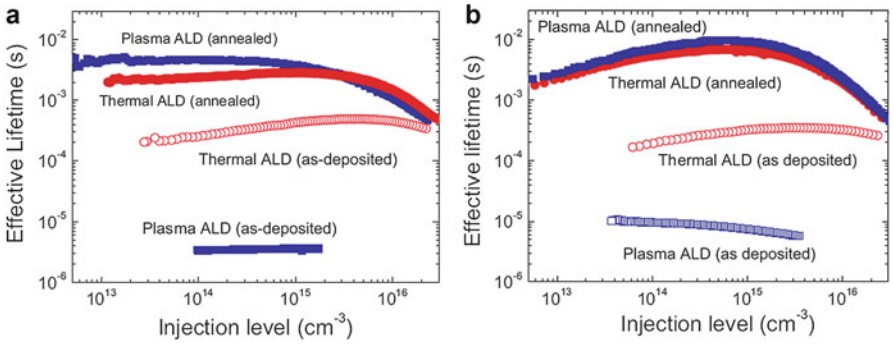


Fig. 1.9 The effective lifetime as a function of the excess carrier density for plasma and thermal ALD-Al_2O_3 before and after annealing (N_2, 400 °C, 10 min) on (**a**) ~2 Ω cm p-type c-Si and (**b**) ~3.5 Ω cm n-type c-Si (Reproducible from Refs. [114, 116]). The wafers underwent a dip in diluted HF prior to being loaded into the deposition chamber. Films with a thickness of ~30 nm were deposited at a substrate temperature of ~200 °C

under formation of methane and O–Al bonds. This reaction is very efficient due to the formation of the strong O–Al bond [107]. The surface chemical reaction during the first half-cycle is similar for plasma and thermal ALD, and can be described by

$$\begin{aligned} &\mathrm{Al-(OH)_2{}^* + Al(CH_3)_3(g) \rightarrow AlO_2 - AlCH_3{}^* + 2CH_4(g)} \quad \text{or} \\ &\mathrm{Al-OH^* + Al(CH_3)_3(g) \rightarrow AlO - Al(CH_3)_2{}^* + CH_4(g)} \end{aligned} \tag{1.6}$$

During the second half-cycle step, the surface changes from methyl-terminated to hydroxyl-terminated. For thermal ALD, the surface chemistry can be summarized by

$$\begin{aligned} &\mathrm{AlO_2 - AlCH_3^* + H_2O(g) \rightarrow AlO_2Al - OH^* + CH_4(g)} \quad \text{or} \\ &\mathrm{AlO - Al(CH_3)_2^* + 2H_2O(g) \rightarrow AlOAl - (OH)_2^* + 2CH_4(g)} \end{aligned} \tag{1.7}$$

For plasma ALD, H_2O and CO_x are produced during the second half-cycle,

$$\begin{aligned} &\mathrm{AlO_2 - AlCH_3^* + 4O \rightarrow AlO_2Al - OH^* + H_2O(g) + CO_x(g)} \quad \text{or} \\ &\mathrm{AlO - Al(CH_3)_2^* + 8O \rightarrow AlOAl - (OH)_2^* + 2H_2O(g) + 2CO_x(g)} \end{aligned} \tag{1.8}$$

It is noteworthy that the formation of the H_2O by-product during the plasma step can lead to a secondary reaction pathway [111].

Both thermal and plasma ALD deposited Al_2O_3 films can provide an excellent level of passivation effect with very low surface recombination velocities $S_{\mathrm{eff}} < 5$ cm/s on low-resistivity p-type and n-type Si (typically, 1–4 Ω cm) after annealing at moderate temperatures [102, 103, 112–115]. Figure 1.9 shows the comparison of passivation performances between plasma and thermal ALD deposited Al_2O_3 by

presenting the injection-level-dependent effective lifetime for Al_2O_3 film deposited on p-type and n-type Si [114, 116]. In the as-deposited state, thermal ALD provides a reasonable level of surface passivation with $S_{eff} \lesssim 30$ cm/s (at an injection level of 10^{15} cm^{-3}) in striking contrast with plasma ALD Al_2O_3 ($S_{eff} \sim 10^3$ cm/s). After annealing at ~400 °C, very high levels of surface passivation with $S_{eff} < 5$ cm/s (p-type Si) and $S_{eff} < 2$ cm/s (n-type Si) were obtained for both ALD methods. In contrast to the as-deposited state, the plasma ALD process afforded a lightly higher level of passivation than the thermal ALD process in the annealing state. These intriguing behaviours can be related to small differences in the level of chemical and field-effect passivation obtained by both methods. For thermal ALD Al_2O_3, the key effect of annealing is the increase of Q_f, whereas for plasma ALD Al_2O_3 the chemical passivation improves dramatically [116–119]. Dingemans et al. [116] reported a relatively low interface defect density (D_{it}) value of ~3×10^{11} eV^{-1} cm^{-2} for the as-deposited thermal ALD Al_2O_3, which is consistent with the moderate level of surface passivation obtained prior to annealing. The boost of surface passivation performance for thermal ALD Al_2O_3 after annealing corresponds to the increase in Q_f at Al_2O_3–Si interface from low values of the order of 10^{11} cm^{-2} to high values of the order of 10^{12} cm^{-2} [116, 119]. However, it has been reported that high Q_f value of 10^{12} cm^{-2} was measured at Al_2O_3–Si interface for plasma ALD in the as-deposited state whereas this method provided a low level of passivation as shown in Fig. 1.9. This low passivation performance is highly related to the high D_{it} values, which may be due to the exposure of the deposited Al_2O_3 surface to vacuum UV radiation that is present in the plasma [116, 120]. After annealing, the interface defect density (D_{it}) can be reduced to a low value of $\leq 1 \times 10^{11}$ eV^{-1} cm^{-2}, which is responsible for the dramatically improved chemical passivation and therefore the high level of surface passivation. For both ALD methods, the Al_2O_3–Si interface after annealing at moderate temperatures features low $D_{it} \leq 1 \times 10^{11}$ eV^{-1} cm^{-2} and high Q_f values in the range of (2–13) $\times 10^{12}$ cm^{-2} [104, 113, 116–120], both of which contribute to efficient surface passivation and thus result in very low surface recombination velocities.

Due to the negative polarity of Q_f at Al_2O_3–Si interface, Al_2O_3 is particularly suitable as a passivation scheme for boron-doped emitters. For example, the ALD synthesized Al_2O_3 films can limit the emitter saturation current density to −10 and −30 fA/cm^2, respectively, for boron doped p^+ emitters with sheet resistances of >100 and 54 Ω/sq [121]. These low saturation current densities imply that a maximum open-circuit voltage (V_{oc}) of up to 700 mV can be obtained for these emitters passivated by Al_2O_3 [112, 122]. One can see from the previous studies [104, 121] that the level of passivation achieved by Al_2O_3 for p^+ surfaces was higher than that obtained by thermal SiO_2 and a-Si:H and significantly higher than that by SiN_x. This can be easily understood due to the differences in strength and polarity of the fixed charges present in the passivation schemes. For n^+ emitters, however, it is expected that the negative Q_f of Al_2O_3 will not contribute to optimal passivation properties when compared to SiN_x containing positive charges. Nevertheless, a recent study [123] shows that implied V_{oc} between 640 and 680 mV can

still be achieved for n^+ emitters with sheet resistances between 20 and 100 Ω/sq using plasma ALD Al_2O_3. The low interface defect density induced by Al_2O_3 as described above may be primarily responsible for this moderate passivation level.

The chemical passivation of Al_2O_3 has been experimentally associated with the hydrogenation of the Al_2O_3–Si interface during annealing [124, 125]. In addition to the interface hydrogenation, the chemical passivation may also be influenced by film relaxation, Si–O bond rearrangements, and some additional interfacial oxide growth during annealing [93]. In the meanwhile, simulations and experiments have provided evidence that the negative charge at Si–Al_2O_3 interface may be related to Al vacancies and interstitial O defects [126–130]. Charge injection phenomenon across the interface may play a role in the formation of the negative charge associated with these defects [130–134]. It is worth stressing that also other mechanisms can contribute to negative charges, and that more research is needed to draw final conclusions.

In order to increase the deposition rate of Al_2O_3 for industrial PV applications, a high-rate ALD concept, namely, spatial ALD equipment has recently been developed [135–138]. It is quite remarkable that the high-rate (typically 14 nm/min) spatial ALD produces exactly the same excellent level of surface passivation as the slow-rate conventional thermal or plasma ALD [119, 139–141]. In addition, two other techniques have recently been demonstrated to be suitable for depositing surface-passivating Al_2O_3 layers. PECVD [113, 142, 143] has been shown to provide S_{eff} of only 10 cm/s on 1 Ω cm p-type Fz-Si, whereas reactive sputtering [144] on comparable material has resulted in S_{eff} down to 55 cm/s. However, these two techniques cannot be applied in high-efficiency Si solar cells due to their relatively lower passivation performances in comparison with ALD.

2.3.5 Amorphous Silicon (a-Si:H)

Hydrogenated amorphous silicon (a-Si:H) is a semiconductor material, in contrast to the above passivation materials that are all dielectric materials. Therefore, in addition to being a passivation scheme, a-Si:H has also been used as the base and emitter materials for Si thin-film solar cells. Here we will not elaborate on Si thin-film solar cells because they are out of the subject of high efficiency due to their lower efficiencies (~10 %) in comparison with c-Si wafer solar cells, although a record efficiency of 13.1 % has been achieved based on a "micromorph" tandem Si thin-film solar cell consisting of a top a-Si:H cell and a bottom microcrystalline Si (μc-Si:H) cell [145]. Furthermore, the a-Si:H films can be n or p-type doped by introducing phosphine (PH_3) or diborane (B_2H_6) as precursor gases together with the silane (SiH_4). As discussed in Sect. 2.2.2, these doped films can be deposited on c-Si wafers as the emitter layers to fabricate Si heterojunction solar cells.

The growth mechanism of a-Si:H has been thoroughly studied and a surface-diffusion scheme has been proposed based on experimental results [146]. It has been demonstrated that SiH_3 radical is dominant chemical species of SiH_4 + H_2 plasma for the growth of a-Si:H [147]. For a-Si:H growth, SiH_3 radical reaching the

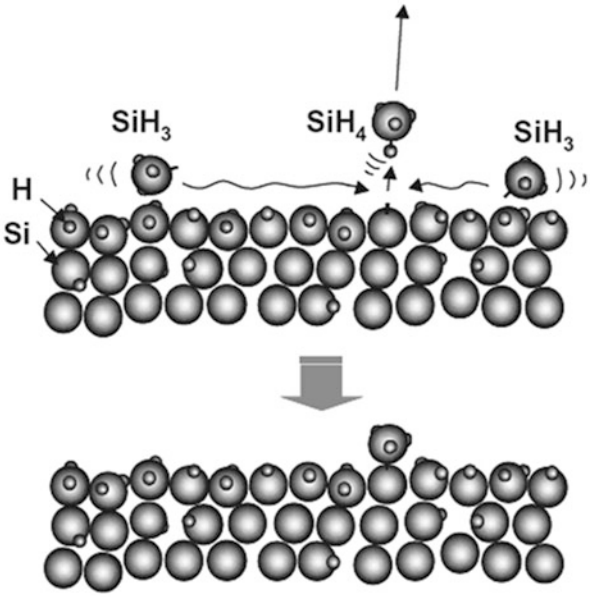


Fig. 1.10 A surface-diffusion scheme for the growth of a-Si:H (reproducible from [147])

film-growing surface starts to diffuse on the surface. During surface diffusion, SiH_3 abstracts surface-covering bonded hydrogen, forming SiH_4 and leaving dangling bond on the surface (growth-site formation). Toward the dangling-bond site on the surface, another SiH_3 diffuses to find the site and to make Si–Si bond (film growth) as schematically shown in Fig. 1.10. In general, besides the adsorbed SiH_3, remaining part of unity-flux density of SiH_3 is reflected by the growing surface. The adsorbed SiH_3 changes its form as follows: (1) SiH_3 abstracts surface-covering bonded H forming SiH_4 or two SiH_3 radicals are encountered on the surface forming Si_2H_6, and (2) surface-diffusing SiH_3 sticks to the dangling-bond site forming Si–Si bond. Once the building unit SiH_3 has sticked to the dangling-bond site forming Si–Si network, further integration becomes ultimately controlled by the self-organization processes on the nanoscale [148]. It is imperative that, depending on the surface-diffusion scheme, the development of a-Si:H thin films be able to proceed through the layer-by-layer growth scenarios [149].

This a-Si:H has been mainly used as a passivation scheme for high-efficiency Si heterojunction solar cells in recent years [150–153]. In order to improve the performance of heterojunction solar cells a thin intrinsic amorphous silicon (i-a-Si:H) is sometimes inserted between the p layer (or n layer) and the n-type (or -p-type) crystalline silicon (the so-called HIT solar cell: heterojunction with intrinsic thin film) [154, 155]. Some other studies [156] have also reported high-efficiency c-Si solar cells using a-Si:H or its stack as the c-Si surface passivation scheme. The passivation principle of amorphous silicon is dominantly based on hydrogen-related chemical passivation. To provide low interface state density at the c-Si–a-Si:H interface good hydrogenation of the interface is critical. Amorphous hydrogenated

silicon (a-Si:H) usually deposited by conventional PECVD at a low temperature of around 225 °C contains a large hydrogen content of >10 % [157], which is responsible for the hydrogenation of the c-Si/a-Si:H interface. Therefore, effective surface recombination velocities of around 2–5 cm/s, which are close to the passivation level of thermally grown oxide, are typically reported in literatures for p-type and n-type wafers with a resistivity of ~1.5 Ω cm [156, 158–163]. In particular, surface recombination values as low as 3 cm/s were achieved in 1.5 Ω cm wafers by a-Si:H grown by conventional PECVD at 225 °C, which were then applied at the rear side to manufacture a 20.1 % efficient crystalline silicon solar cell [156]. Amorphous silicon can be also deposited by HWCVD and ICP CVD. For example, Muñoz et al. reported implied open circuit voltage near 700 mV after surface passivation of p-type 0.8 Ω cm wafers, with S_{eff} around 15 cm/s [164]. In our published work [47, 165], we used a remote ICP system to deposit a-Si:H films and obtained S_{eff} of 30 cm/s after surface passivation of p-type 1–2 Ω cm Cz-Si wafers. Recently, we have also developed a novel capacitive-coupled electrode-less plasma (CCEP) system based on ICP for the deposition of a-Si:H films and obtained S_{eff} as low as 5 cm/s [166].

The excellent passivation properties of a-Si:H deposited at low temperature advance the development of HIT solar cells and a record high efficiency of 23.0 % on HIT solar cells has been achieved by SANYO LTD [167, 168]. However, for industrial c-Si wafer solar cells, there are some limitations of the application of a-Si:H surface passivation films, such as parasitic absorption effect and the lack of thermal stability during high-temperature processes (such as contact firing). The former is related to the strong absorption of a-Si:H for photon energies above the bandgap $E_g = 1.7$ eV [169]. This problem can be solved by tuning the thickness of a-Si:H films to achieve the optimum of transmission and passivation [170]. The latter is associated with the structural properties of a-Si:H. At a high temperature of >450 °C, high hydrogen effusion from the a-Si:H film may occur due to the high mobility of this atom or molecule, leaving remaining dangling bonds at the interface and therefore diminishing the surface passivation quality [171]. Introducing a cap layer (like SiN_x) on the a-Si:H surface (namely, using passivation layer stacks) could lead to more stable films under post annealing effects [158, 159, 171]. The cap layer acts as a diffusion barrier for hydrogen and thus avoid the effusion of hydrogen out of a-Si:H films. In addition, if the cap layer is transparent then it could be applied as an antireflective layer (like SiN_x) at the front side of the solar cell. In this case, the thickness of a-Si:H film can be optimized so that parasitic absorption will be minimized consequently.

2.4 Other Functional Materials

Other functional materials for high-efficiency silicon solar cells include antireflective materials, metal electrode materials, and transparent conductive materials. For high-efficiency c-Si wafer solar cells, SiN_x is the dominant material

as the antireflective layer whether it being a whole passivation scheme simultaneously or being a part of passivation stacks because SiN_x is transparent to sun light and provides a good passivation performance with a tunable refractive index in the range of 1.9 ~ 2.8 [93]. In some other cases, thermally grown SiO_2 can also be used as the antireflection and passivation scheme for high-efficiency Si wafer solar cells since it is transparent to sun light and has an excellent passivation performance with an appropriate refractive index of 1.46. The metal electrode materials generally refer to screen-printed aluminium or silver pastes, ion-beam evaporation deposited aluminium or silver layers, superlattices such as Ti/Pd/Ag and so on. The transparent conductive materials are only used in high-efficiency HIT solar cells. For HIT solar cells, the lateral conductivity of the thin dope a-Si:H layers (emitters) is rather poor, so transparent conductive oxide (TCO) layers are deposited on the a-Si:H films. Ideally, these TCO layers simultaneously guarantee lateral charge transport to the external metal contacts, low contact resistance to the underlying doped a-Si:H layers, and maximal optical transmission into the active absorber, i.e. the c-Si wafer. Indium tin oxide (ITO) and zinc oxide (ZnO) are often the choice of TCO materials in HIT solar cell devices and are usually deposited by reactive magnetron sputtering.

3 High-Efficiency Solar Cell Devices

3.1 Passivated Emitter and Rear Cell (PERC)

In this section, we elaborate on high-efficiency PERC devices, which are a developed and improved design of industrial standard screen-printed p-type Si solar cells. As described above, the full-area Al BSF exhibits only a moderate passivation quality for industrial standard screen-printed p-type Si solar cells. In addition, only about 70 % of the infrared light reaching the aluminium rear contact is reflected back into the silicon wafer [172]. These electrical and optical losses can be reduced by applying the passivated emitter and rear cell (PERC) solar cell design [71], as shown in Fig. 1.11. At the cell rear, a significantly improved surface passivation and optical reflectivity are achieved by dielectric layers compared with the full-area Al-BSF. The adaptation from the standard Al-BSF cell to a PERC cell requires local contact formation by, for example, laser processing [173, 174]. Among all dielectric layers discussed above, ALD-deposited Al_2O_3 and thermally grown SiO_2 are most outstanding for the rear side passivation of PERC cells in consideration of the base polarity (p-type). In general, passivation layer stacks such as Al_2O_3/SiN_x or SiO_2/SiN_x are applied as the rear side passivation scheme for high-efficiency PERC cells. We will discuss the role of SiN_x capping layer in the following context.

The detailed fabrication process of PERC cells is slightly different from that of industrial standard Al-BSF cells. Before texturing and phosphorus diffusion, a dielectric protection layer such as SiN_x is deposited on the rear side of the solar

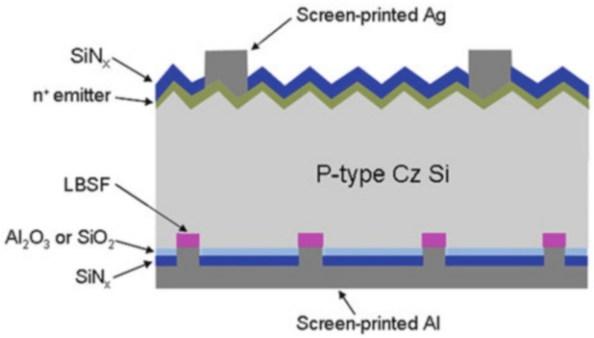


Fig. 1.11 A scheme of the PERC solar cells with screen-printed front and rear contacts with Al_2O_3/SiN_x or SiO_2/SiN_x rear passivation stacks. LBSF represents local back surface field

cell. The dielectric layer plays as a barrier against the alkaline texturing process and the phosphorus diffusion. Therefore, only the front side of the solar cell is textured and phosphorus doped, whereas the rear side remains planar and boron doped. The HF etch after the diffusion step is slightly adjusted in order to remove the dielectric layer at the rear in addition to the phosphorus silicate glass (PSG) at the front. Afterwards, a 10-nm ALD-deposited Al_2O_3 layer is deposited or a dry thermal oxidation is carried out resulting in a 10-nm-thick SiO_2 layer on both the rear surface and the front surface. This SiO_2 layer capped by a following deposited SiN_x layer on the front surface can provide a better passivation performance than the single SiN_x layer. Subsequently, a PECVD-SiN_x with a refractive index of $n = 2.05$ and a thickness of about 200 nm is deposited at the rear. The SiN_x capping layer at the rear serves in several roles: (1) it decreases the surface recombination velocity after the firing process of the rear passivation layer for both Al_2O_3 [115] as well as SiO_2 [175]; (2) it protects the 10-nm thin rear surface passivation layer from being etched by the Al paste during the firing process; and (3) it improves the internal optical reflectance of the rear side [176]. The front side is then coated with a 80-nm-thick SiN_x layer. However, for the SiO_2-passivated PERC cell, the SiN_x thickness is slightly reduced in order to compensate the 10-nm thin SiO_2 at the front and achieve good antireflection properties. Then, the dielectric passivation layer stacks at the rear side are locally ablated by laser contact opening using a pulsed laser to form local line openings. Finally, a screen-printing process on both the front side and rear side followed by a firing step promotes the formation of local Al-BSF and thus finalizes the PERC cell.

In a recent study on high-efficiency PERC cells (p-type Cz Si) [176], Dullweber et al. compared the reflectance and internal quantum efficiency (IQE) between PERC and Al-BSF solar cells, as shown in Fig. 1.12. In the long wavelength region $l > 900$ nm, the dielectric rear surface passivation strongly improves the reflectivity and the IQE. In the inserted table, the $S_{\text{eff, rear}}$ and the internal reflectance R_{rear} are also shown, extracted from the data in the long wavelength region using the software LASSIE [177]. The obtained $S_{\text{eff, rear}}$ values of 70 ± 30 cm/s and

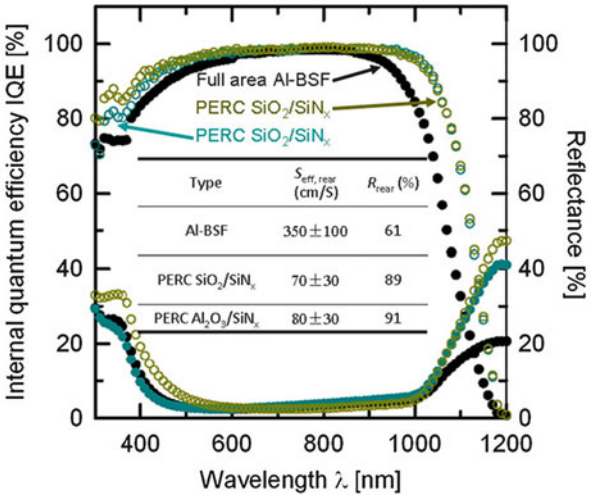


Fig. 1.12 Comparison of internal quantum efficiency (IQE) and reflectance between PERC solar cells with SiO_2/SiN_x and Al_2O_3/SiN_x passivation stacks at the rear and a full-area Al BSF reference cell. The *inset table* shows the rear surface recombination velocity $S_{\text{eff, rear}}$ and internal reflectance R_{rear} of the Al-BSF cell and the PERC cells with dielectric passivation stacks at the rear. (Reproducible from [176])

80 ± 30 cm/s for SiO_2-passivated and Al_2O_3-passivated PERC cells, respectively, are obviously far smaller than that (350 ± 100 cm/s) for Al-BSF solar cells, indicating a much stronger passivation effect of the dielectric layers than that of Al-BSF. Both the IQE and reflectance results suggest that the dielectric rear surface passivation can provide a higher reflectance especially in the long wavelength region. In particular, they have achieved a high efficiency of 19.0 % and an enhanced efficiency up to 19.4 % for the PERC cell with Al_2O_3/SiN_x passivation stacks and the one with SiO_2/SiN_x passivation stacks, respectively.

In the very early time of 1989, a record efficiency of 22.8 % was obtained by Blakers et al. [71] for small-area PERC solar cells based on p-type Fz Si substrates. This strong gain in efficiency can be ascribed to the higher bulk lifetime of Fz Si substrates in comparison with that of Cz Si substrates. In other reports [178–180], high conversion efficiencies up to 19.6 % has been achieved for large-area screen-printed PERC solar cells based on p-type Cz Si substrates. Recently, a novel print-on-print (PoP) process has been considered as a technological improvement that should enable conversion efficiencies of up to 20 % for PERC silicon solar cells (p-type Cz Si substrates) in the near future [176]. For the PoP process, the Ag front contact is deposited in two consecutive screen-printing steps using a DEK PVP1200 printer. In this case, the number of fingers has been increased from 50 for standard single print to 60 for PoP in order to minimize resistive losses due to the significantly smaller finger width. Also the shadowing loss can be reduced, resulting in a higher short-circuit current density. Another technology is the use of Physical Vapour Deposition (PVD) for the metallization of PERC cells instead of the

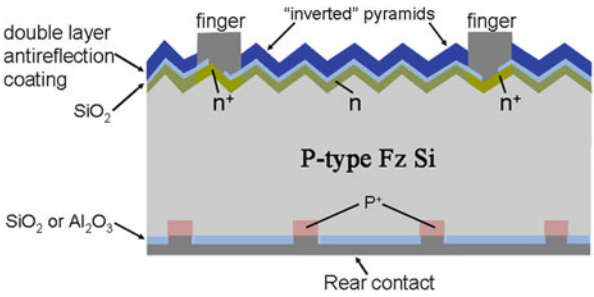


Fig. 1.13 A schematic structure of the Passivated emitter, rear locally diffused (PERL) cells

standard screen printing of metal pastes for establishing either the complete metallization or a seed layer for subsequent electroplating. Less shadowing and a lower contact resistance are compared to screen printed contacts the two major advantages of sputtered contacts. Using this in-line sputtering technology, the Fraunhofer Institute for Solar Energy Systems (Germany) manufactured large scale (125 × 125 mm^2) PERC0020cells based on Fz Si substrates with a high efficiency of 21.1 % [181]. Efficiencies of small-area p-type multi-Si solar cells exceeding 18 % with Al BSF [182] or silicon nitride [183] have been reported, but a much better result of 19.8 % has been achieved by PERC concepts with "honeycomb" textured front surface and thermally grown SiO_2 passivation scheme [184]. However, the high-temperature oxidation (more than 1,000 °C) [185, 186] leads to the significant reduction of minority-carrier lifetime in multi-Si, and thus degrades the efficiency. This thermal degradation can be prevented by lowering the process temperature to 800 °C during wet oxidation of the rear surface. Using this process, Schultz et al. [187] demonstrated conversion efficiencies of 20.3 % for multi-Si and 21.2 % for FZ-Si PERC silicon solar cells on small device areas (1 cm^2).

3.2 Passivated Emitter, Rear Locally Diffused (PERL) and Passivated Emitter, Rear Totally Diffused (PERT) Cells

The passivated emitter cell series, particularly the PERL (passivated emitter, rear locally diffused) cells, developed at the University of New South Wales, have made major contributions to the development of high-efficiency silicon solar cells [78, 79, 188–192]. Figure 1.13 shows the schematic structure of PERL cells. In pursuit of the highest cell efficiencies, high carrier lifetime p-type Fz silicon wafers of 1.0 Ω cm resistivity and 450 μm thickness were often used as the base material for these PERL cells [188–190, 193]. Both the front and rear surface can be passivated and almost completely enshrouded by thermally grown SiO_2, while the rear surface (p^+) also can be passivated by ALD-deposited Al_2O_3. This oxide reduces recombination along cell surfaces, improving both the collection probability for carriers generated near the surface and the open-circuit voltage. Metal contact to the cell rear is made through small holes in this oxide by laser opening to keep the contact

area as small as possible due to the inferior recombination properties of the contact region. Immediately beneath these rear contact areas, the silicon is heavily doped (with boron) to further suppress contact recombination by providing a field-effect passivation effect and suppressing minority carrier concentrations. Such local $p–p^+$ high–low junction provides a better passivation performance than the local Al-BSF as used in PERC cells. A high lifetime BBr_3 boron diffusion was specially developed for such cell processing [78, 79, 193]. The top surface contact was made via a contact stripe through the oxide to further reduce the recombination loss at this contact. The front contact areas were also further passivated by a heavily phosphorus diffused area. The distribution of emitter layer consisting of heavily doped region (n^+) beneath the contact area and routinely doped region (n) at the non-metallized area is the so-called selective emitter (SE) design [194], which is high on the roadmap list towards high-efficiency Si solar cells.

Apart from the above features that induce almost complete surface passivation and the formation of SE, the incorporation of an efficient rear surface mirror formed by the rear aluminium layer displaced from the silicon surface by the intervening oxide gives a high internal surface reflectance for all internal angles of incidence of light onto this stack. Furthermore, the "inverted pyramid" texture on the front surface by anisotropic etching of the originally (100) orientated surface not only reduces the external surface reflection by giving the incident light two chances to enter, but also gives a high internal reflection for the light reflected from the rear surface. In this way, weakly absorbed light can be trapped in the cell for an average path length enhancement of about 40 times for the present devices [195]. The antireflection coating can be simply single layer such as SiN_x or double layers consisting of two SiN_x layers with different refractive indexes as well as MgF_2/ZnS stacks.

In particular, Zhao et al. at the University of New South Wales fabricated PERL cells based on both multi-Si and Fz-Si materials using thermally grown SiO_2 as the whole passivation scheme and MgF_2/ZnS double layer as the antireflection coating [189]. The "inverted-pyramid" surface texturing of Fz mono-Si substrates is not applicable to multi-Si substrates since it relies on anisotropic etching of the originally (100) orientated surface. Therefore, the authors used a masking oxide with uniformly distributed holes to fabricate honeycomb texture surfaces on multi-Si substrates by isotropic etching through these holes. The insert table in Fig. 1.14 compares the independently confirmed performance of the honeycomb multi-Si PERL cell to both an untextured multi-Si PERL cell and a high-performance Fz mono-Si PERL cell. The latter demonstrates an ultrahigh performance of 24.4 % with extremely high open-circuit voltage of 696 mV, short-circuit current of 42 mA/cm^2 and fill factor of 83.6 %. The textured multi-Si PERL cell also moves into high-efficiency Si solar cell class since it exhibits a high efficiency of 19.8 % in comparison with the untextured multi-Si PERL cell.

As the wavelength dependent reflection and external quantum efficiency (EQE) of the three cells show (see Fig. 1.14), honeycomb texturing results in reflection generally intermediate between that of untextured cell and the inverted-pyramid cell. At the longest wavelengths, silicon becomes transparent and reflection from all three devices increases. The lower reflection from the textured sample results from

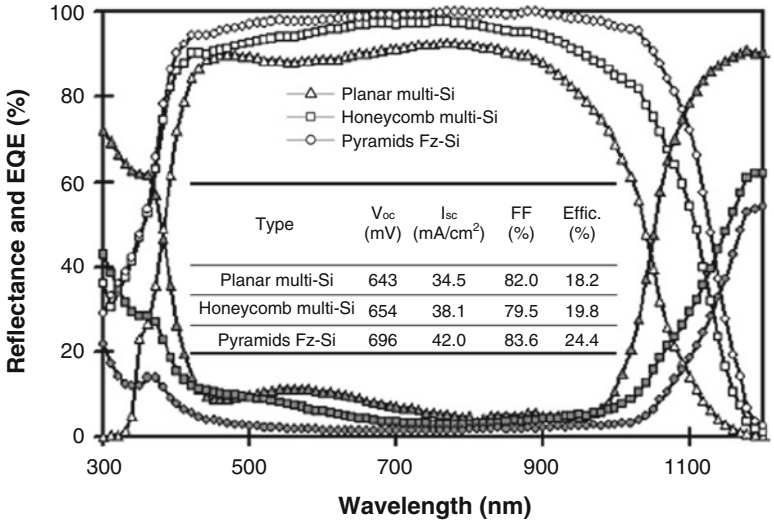


Fig. 1.14 Reflection (*lower curves*) and external quantum efficiency (*upper curves*) as a function of wavelength for the three cells: planar multi-Si PERL cell, honeycomb multi-Si PERL cell and pyramids Fz-Si PERL cell. The *inset table* presents the performances including open-circuit voltage, short-circuit current, fill factor and efficiency of the three PERL cells. Cell area is 1 cm^2 for multi-Si cells and 4 cm^2 for Fz mono-Si device, respectively. Measurements are carried out under standard test conditions (Global AM1.5 spectrum, 100 mW/cm^2 intensity, 25 °C cell temperature). (Reproducible from [189])

increased absorption in this rear reflector due to multiple light passes across the cell. The results suggest light trapping in the honeycomb textured cell is comparably effective to that in inverted-pyramid cells. From overall prospective, the planar cell suffers considerably in reflection and EQE due to poor light trapping. The difference at shorted wavelengths between the textured cells are primarily due to marginally superior optical performance of the inverted-pyramid scheme augmented by the better quality of the Fz monocrystalline material, which ensures that essentially every photogenerated carrier is collected.

In fact, the record efficiencies of small area (4 cm^2) PERL cells on Fz (1 Ω cm) and MCZ (~5 Ω cm) Si substrates have been updated to 24.7 % and 23.5 % [190], respectively. The slightly lower efficiency of MCZ Si PERL cells may be related to the fact that many of these MCZ substrates have higher resistivities than those of Fz wafers, and hence giving relatively lower fill factors on such high resistivity wafers due to the current crowding effect at the low coverage small rear contact areas [196]. To reduce this current crowding effect and to improve the cell fill factors, a PERT (passivated emitter, rear totally diffused) cell structure was designed [79, 190–192]. As shown in Fig. 1.15, the PERT cell has added one more processing step to diffuse a light boron layer along the entire rear surface of the cell, while all the other features of the PERL cells remain. The conducting p-type layer totally diffused along the rear surface is expected to supply a low resistance path whereby the photo-generated holes move vertically towards this layer, and then move

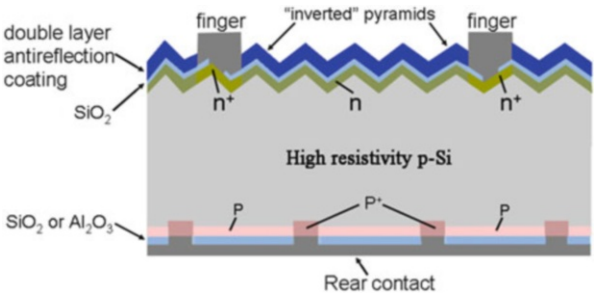


Fig. 1.15 Passivated emitter, rear totally diffused (PERT) cell structure

through this diffused layer laterally towards the rear contact windows with minimum resistance loss. This total rear diffusion had also to be compromised between high conductivity and low rear surface recombination velocities. Hence, it was made with a lower boron doping level than the local boron diffusion regions, which were required for passivation of the high recombination rear metal contact.

The PERT structure was firstly reported to improve the fill factors for very-high-resistivity substrates of 100 Ω cm in the early stages of the PERL cell development in early 1991 [197]. In two representative reports [190, 192], for MCZ substrates with a high resistivity of ~5 Ω cm, the small area (4 cm^2) PERL cells exhibit a relatively lower fill factor of 81.1 % and a lower efficiency of 23.5 % than the corresponding small area (4 cm^2) PERT cells with a fill factor of 83.5 % and a high efficiency of 24.5 %, although their open-circuit voltages and short-circuit currents are almost the same. The remarkable 24.5 % efficiency is the highest ever reported efficiency for a silicon cell made on MCZ Si substrate. However, for small area PERL and PERT cells on p-type Cz Si substrates, the maximum efficiency can only reach about 21 % [191, 192].

Apart from p-type substrates, PERL and PERT cells can also be fabricated on n-type substrates. An Al_2O_3/SiN_x stack was used on the front boron-diffused emitter while the back side is still passivated by thermally grown SiO_2 [106]. For n-type Fz Si PERL cells, Benick et al. in Fraunhofer ISE reported record efficiencies of, at that time, 23.2 % (V_{oc} = 703 mV, J_{sc} = 41.2 mA/cm^2, FF = 80.2 %) [106]. In a subsequent work, the efficiency was even improved further to 23.9 % (V_{oc} = 705 mV, J_{sc} = 41.1 mA/cm^2, FF = 82.5 %) [105]. Internal quantum efficiencies of approximately 100 % were obtained for the front side, in combination with V_{oc} values >700 mV. The n-type PERL cell, featuring local n^+ BSFs fabricated using photolithography processes, presents a complex cell concept involving many different process steps. To simply the formation of the n^+ BSF, a novel process was developed at Fraunhofer ISE where a phosphorous containing passivation layer (called PassDop) is locally opened by a laser under the simultaneous diffusion of P atoms into Si. Using this process, promising efficiencies of 22.4 % have already been demonstrated on Fz n-type Si PERL cells [198]. In recent studies [199], Glunz et al. fabricated small area (4 cm^2) n-type PERT cells using Al_2O_3/SiN_x stacks as the front passivation scheme and full metallization of n^+ diffused rear side, and obtained efficiencies of 20.8 % and 19.4 % for 1 Ω cm Fz and Cz substrates, respectively.

3.3 Pluto-PERC and Pluto-PERL Cells (Full-Scale Commercialization)

Among the emerging high-efficiency cell designs, the concept of the SE appears to be the most eagerly pursued approach for commercial application in recent times [200]. Various innovative SE technologies such as doped Si inks [201, 202], oxide mask process [203], ion implantation process [204], etch-back process [205] and laser doping [206–210] have been developed which have demonstrated an average efficiency of 18.5 % in pilot or full-scale Cz mono-Si cell production. Also employing the SE concept is the Pluto cell technology developed by Suntech Power in collaboration with the University of New South Wales [211] based on the world-record holding PERL cell structure [188, 190, 212]. Pluto achieves an average cell efficiency of ~19 % in a 0.5 GW production, with highest efficiency of 19.6 % independently confirmed [213, 214]. This result translates to a 5–10 % boost in efficiency, when directly compared with standard screen-printed cells. However, device loss analysis has indicated that the full Al-BSF at the rear surface accounts for over 50 % of the total dark saturation current of the Pluto cell [215, 216]. This finding clearly reveals that changes and improvements to the rear surface design by incorporating further attributes of PERC or PERL cells may further enhance the cell efficiency. Earlier in 2011, a new record of 19.7 % [214] was independently confirmed by Solar Energy Research Institute for a Pluto cell using the Pluto-PERC cell structure and the same commercial p-type Cz mono-Si wafers. More recently, an efficiency of 20.3 % has again been independently confirmed by SERIS on similar commercial-grade Cz mono-Si wafers, this time using the Pluto-PERL structure [217].

In comparison with PERL cells developed by the University of New South Wales, the Pluto-PERL cells used solar grade p-type Cz wafers instead of high-quality Fz wafers. Also the double-layer antireflection coating is replaced by single layer antireflection coating, namely, SiN_x. The inverted pyramids texture developed by photolithographic texturing is also replaced by upright pyramid texture fabricated by anisotropic etching. Reflection from this surface is below that of the inverted pyramids texture due to the elimination of the flats between adjacent inverted pyramids. This cancels out the loss resulting from the use of a single layer antireflection coating. The effective surface recombination velocity however of the upright pyramids when diffused and passivated with SiN_x is not quite as good as for the photolithographically defined inverted pyramids leading to the loss of several mV in open circuit voltage when the V_{oc} is exceeding 700 mV, but leading to negligible loss when used in conjunction with Cz wafers where the V_{oc} is only in the vicinity of 660 mV. Innovative patterning techniques for the silicon nitride have alleviated the need for both high-temperature thermal oxidations and photolithographic/mask aligning processes. The complicated and expensive metallization scheme consisting of evaporated Ti/Pd/Ag metal contacts have been replaced by a simple, low-cost, high-throughput self-aligned metallization technique. When used in conjunction with the above silicon nitride patterning techniques, metal

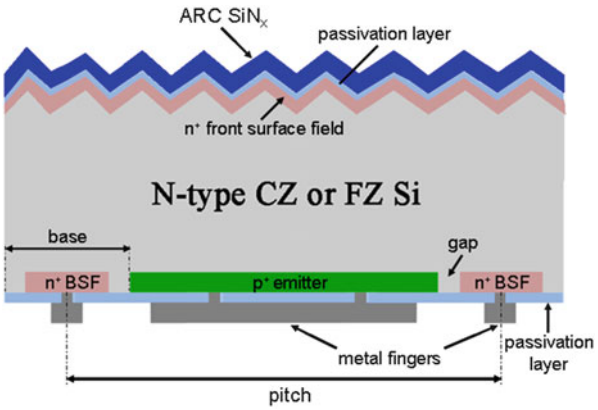


Fig. 1.16 Schematic of an IBC cell, indicating the n^+-Front Surface Field (FSF), n^+-BSF, p^+-emitter, contacts and passivation layers. The definition of pitch, base and gap are also included (The pitch size is the sum of the emitter size and the base size). All contacts are located at the rear

lines comparable in width and conductivity with the photolithographically defined Ti/Pd/Ag metal contacts have been achieved and implemented into large scale production with full size commercial substrates. This important transition was achieved with no performance loss compared to the PERL cells. A 5 % power loss for the Pluto-PERL cells resulted from scaling the typical size (2×2 cm^2) to that (12.5×12.5 cm^2) used commercially. This was contributed to by a 2 % loss in short circuit current resulting from the increased metal shading loss and a 3.4 % loss in fill factor [213]. The combined efficiency losses associated with all of the above correspond to a performance loss of 17.3 % for the large area Cz Pluto-PERL cell compared to the small area laboratory type Fz PERL cell. This translates to a reduction in efficiency from approximately 25 % to about 20.5 % [213].

3.4 Interdigitated Back-Contact (IBC) Cells

Interdigitated back-contact (IBC) silicon solar cells become more and more attractive for the industry mass production because of its high-efficiency potential and simple cell interconnection in modules [218]. The main structure differences are the location of the emitter and its contact, which is on the rear for the IBC cell instead of the front for the industrial standard p-type silicon solar cells. For the IBC cell, the emitter and the BSF dopings are both located in an interdigitated structure on the back side of the solar cell, as shown in Fig. 1.16. Thus, both metallization grids are also located at the rear side of the cell. The IBC solar cell has many advantages. The most prominent one is the adoption of all rear contacts, which eliminates optical shading losses at the front side. Therefore, this cell type has an increased absorption and short circuit current density. One more advantage is the

possibility of wide emitter and base metallization fingers at the rear side of the cell to reduce the series resistance of the metal contacts. In general, these IBC cells are mainly fabricated on n-type Si wafers with boron-diffused emitters since n-type Si material has been proved to be more suitable for IBC solar cells due to its larger tolerance to most common impurities compared to p-type Si [219]. Moreover, n-type CZ Si is free of light-induced degradation related to boron–oxygen complexes, which is often seen in p-type CZ Si material.

The fabrication process of IBC cell usually involves the following sequences. First, to enable an optimal light trapping, the front surface of n-type CZ (or FZ) silicon wafers is textured with random pyramids while the rear surface is polished. Second, the front surface field (FSF) and BSF are formed separately by $POCl_3$ diffusion. Subsequently, the rear emitter pattern is defined by lithography and formed by locally etching the BSF region. This is followed by rear boron diffusion to create p^+-emitter or screen-printing and firing of aluminium paste to create Al-alloyed p^+-emitter. Then, a front surface passivation layer followed by an antireflection coating layer (usually single SiN_x layer or SiO_2/SiN_x stack) is deposited at the front. Meanwhile, a passivation layer (usually single SiO_2 layer or SiO_2/SiN_x stack) is also deposited on the rear. Later on, all the rear contact holes are opened by lithography, and metal contacts are applied by screen-printing or e-beam evaporation.

For IBC cells, the FSF acts as an electrical field that repels the minority carriers at the front surface and thus reduces the front surface recombination [220]. Furthermore, the FSF strongly improves the stability of the passivation quality under UV-light exposure [221]. Finally, solar cells with FSF show a linear current response under low-illumination conditions [222]. In a recent study published by Gong et al. [223], the authors investigated the performance dependence of IBC cells on three different FSF-doping profiles and came to a conclusion that the optimum short-circuit current density (J_{sc}) is expected for the shallowest profile with a low surface concentration.

Many experimental and simulated results [218, 221, 223–231] have shown that the IBC cell performance significantly depends on the pitch size and the emitter fraction (namely, the ratio of the emitter size to the pitch size). Higher J_{sc} values were found for larger emitter fractions and thus a larger current collecting area [223, 228, 229]. In a recent simulation study based on 150-μm-thick n-type FZ wafers with a resistivity of 1 or 8 Ω cm [224], Kluska et al. in Fraunhofer Institute for Solar Energy Systems (ISE) mainly attributed the loss of cell efficiency to both the electrical shading effects on the short circuit current density for small emitter coverage and series resistance losses for large emitter coverage, as shown in Fig. 1.17 (reproducible from [224]). Therefore, the maximum cell efficiencies for the typical IBC cell designs have en emitter fraction between 70 and 80 %, which determines the optimum balance between these two losses. Furthermore, the graphs show the positive influence of an increasing base resistivity on the electrical shading losses as well as its negative effect on the series resistance losses. The positive influence of a rising base resistivity can be seen in the decreasing slope of the cell efficiencies that are limited by electrical shading losses. On the other hand

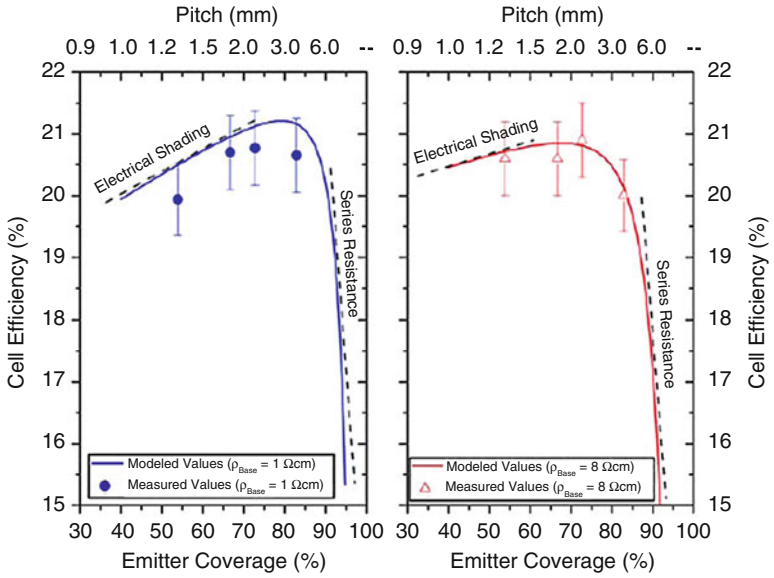


Fig. 1.17 Modeled and measured cell efficiencies for a varying emitter coverage and a constant base width of 600 μm. The maximum cell efficiency is a balance between the limiting electrical shading losses and series resistance losses. The error bars are caused by measurement errors. Note that the upper scale of the pitch is not linear. (Reproducible from [224])

the rising base resistivity leads to more series resistance losses, which cause an early decrease of the maximum cell efficiency for large emitter fractions. The same group in Fraunhofer ISE [228, 229] also experimentally demonstrated maximum efficiencies of 21.3 % and 20.7 % on 1 Ω cm and 8 Ω cm FZ wafers, respectively for those IBC cells with a pitch of 1,800 μm and an emitter fraction of 67 %. In another experimental investigation based on 2–3 Ω cm 300-μm-thick n-type FZ and 2 Ω cm 200-μm-thick n-type CZ Si wafers [223], the best cells with an efficiency of 19.1 % were those with smallest pitch (1,600 μm) and largest emitter fraction (85.7 %).

Several dielectric layers or stacks such as SiN_x, SiO_2, Al_2O_3 and their stacks have been tested for their passivation on both the front and rear surface of the IBC cells [218, 220, 223, 226, 229, 232–234]. In a recent paper, Sunpower Corp. has demonstrated a record efficiency of 24.2 % based on large area (155.1 cm^2) IBC cell designs using n-type FZ wafers and thermally grown-SiO_2 passivation scheme [232]. To date Sunpower Corp. worldwide have successfully implemented their proprietary fabrication approach and industrial feasible patterning techniques in large scale CZ Si IBC cell manufacturing with an average efficiency above 22 % [218]. By applying ALD-Al_2O_3 and PECVD-SiO_x films to the small-area (4 cm^2) IBC cells based on 1 Ω cm 200-μm-thick n-type FZ Si wafers, Reichel et al. [234] in Fraunhofer ISE have achieved an efficiency of 22.7 % (V_{oc} = 706 mV, J_{sc} = 41.0 mA/cm^2, FF = 78.5 %). Other groups also investigated low-cost approaches using currently well-established manufacturing process technologies, such as

wet-processing, tube furnace diffusion, PECVD and screen printing for metallization and patterning, as well as screen-printed Al-alloyed p^+ emitter. Since 2009, Siliken has been building a pilot production line to explore both mainstream and alternative cost-effective processing approaches that can be scaled to production while reaching stabilized efficiencies beyond the 20 % benchmark for CZ Si IBC cells [226]. In a recent study, Bock et al. [233] developed IBC cells using screen-printed Al-alloyed p^+ emitter and Al_2O_3 as the rear passivation scheme and achieved an efficiency of 19.0 % on 1.8 Ω cm 150-μm-thick n-type FZ wafers. In addition to the n-type Si wafers, IBC cells can also be fabricated on p-type FZ Si wafers. In 2007, Engelhart et al. [220] fabricated the Rear Interdigitated contact scheme through a Single Evaporation (RISE) process and demonstrated an independently confirmed efficiency of 22.0 % for IBC cells on 1.5 Ω cm 300-μm-thick p-type FZ wafers.

3.5 Emitter-Wrap-Through (EWT) and Metallization-Wrap-Through (MWT) Cells

The concept of Emitter-Wrap-Through (EWT) solar cell was first introduced by Gee et al. [235, 236] and then demonstrated by Glunz et al. [237] reporting a cell efficiency of 21.4 % on an area 4 cm^2 on high-quality material (FZ Si) using PVD for metallization and photolithography as masking technology. As shown in Fig. 1.18, the EWT cell has an emitter at both the front and rear side, but the metal contacts are restricted to the rear, so the front emitter should be connected by a large number of laser-drilled and emitter-diffused via-holes with the rear side emitter. As in the case of IBC cells, the rear side emitter covers a significant fraction of the rear side commonly with interdigitated doping and metallization structure. The advantages of the EWT solar cell are comparable to the ones of IBC cells: (1) complete elimination of optical shading losses at the front side; and (2) the possibility of the coplanar interconnection of metal contacts. However there exists one major advantage of the EWT cells over IBC cells. Due to the presence of emitter on both the front and rear sides, some of the photo-generated minority carriers in the base diffuse to the front emitter, where they become majority carriers and drift through the EWT via-holes to the rear emitter. The other minority carriers diffuse directly to the rear emitter. In this situation, the average distance of the photo-generated minority carriers to the emitter is significantly reduced. This results in the much lower required minority carrier lifetime in the base than in the case of IBC cells. Therefore high current densities can be collected and thus high efficiency can be achieved in this cell structure with medium quality base silicon in comparison with IBC cell structures.

The fabrication process of EWT solar cells usually involves several delicate technologies, such as physical vapour deposition (PVD) for metallization, photolithography as masking technology and laser technology for drilling holes and local

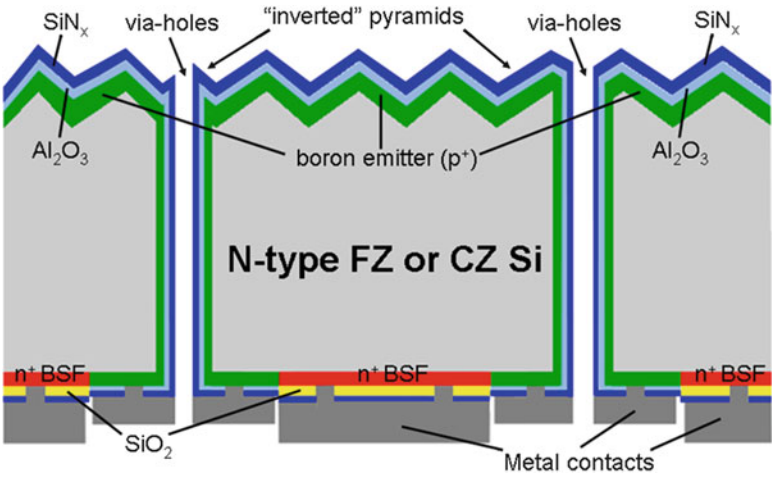


Fig. 1.18 A representative cross-sectional scheme of the n-type FZ or CZ Si EWT solar cells with passivation schemes covering all the Si surfaces: the front side, the rear side and the via-holes. In general, the passivation schemes usually cover only the front and rear surfaces for most Si EWT solar cells

contact openings. Figure 1.19 is a representative processing sequence of p-type CZ-Si EWT solar cells (reproducible from [238]). A detailed description of the process sequence can also be found in [239–241].

(a) After a standard cleaning step, a wet thermal oxidation at 1,000 °C is performed.
(b) The SiO_2 is chemically removed from the intended front side to permit texturing using random pyramids.
(c) After the alkaline texturing, a SiN_x protection layer is deposited onto the textured front side by means of PECVD. Laser technology is then used to locally ablate the SiO_2 layer on the rear side in an interdigitated pattern with photolithography defining the rear side emitter regions. In the meantime, via-holes are also drilled through the wafer using laser technology. The laser-induced damage caused by both processes is subsequently removed by means of a wet-chemical etching step in a KOH solution. During the damage etch, the remaining SiO_2 layer on the rear side acts as an etch barrier leading to the two-level rear side structure of the cell as shown in Fig. 1.19.
(d) The front side is protected by the SiN_x-coating, which is removed from the wafer after etching. Following that, in a conventional $POCl_3$ diffusion step at 880 °C, the phosphorus-emitter is formed in the inner wall of the via-holes, on the full textured front side area and at the laser structured and damage etched rear side areas. On the elevated areas of the rear surface the SiO_2 layer acts as a diffusion barrier and thus defines the base structure of the cell.
(e) Anti-reflection properties and an excellent front surface passivation are achieved by depositing a PECVD-SiN_x.

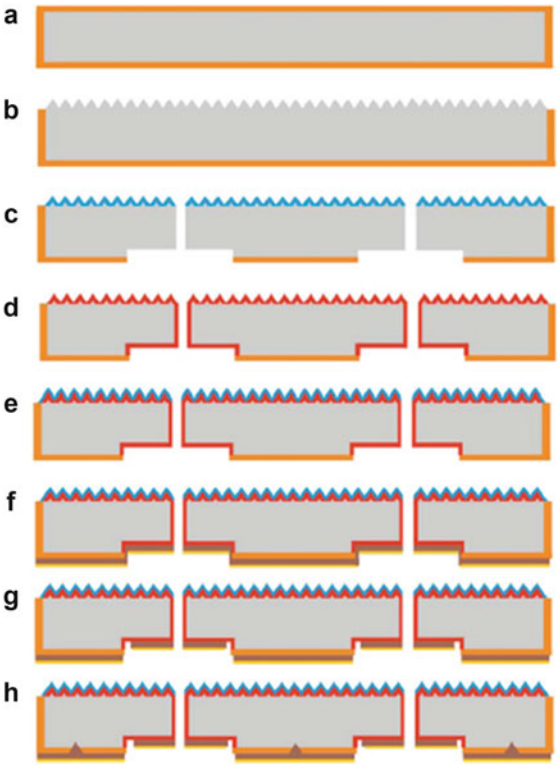
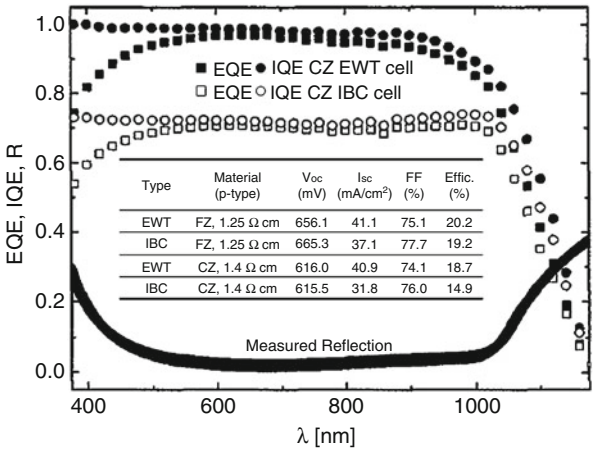


Fig. 1.19 A representative fabrication sequence of the p-type CZ-Si EWT solar cells. (Reproducible from [238])

(f) At the rear, a 10 μm thick Al layer is evaporated, followed by a 300 nm thin layer of SiO_x, which acts as an etching barrier.
(g) The flanks between emitter and base are selectively etched off [242] because they are less protected by the SiO_x layer, due to its columnar growth. This separates the emitter from the base regions.
(h) Finally, local base contacts are formed by laser firing.

According to the above discussion, the EWT cells usually exhibit a better performance on medium-quality Si substrates than IBC cells. In early 2003, Kray et al. [243] from Fraunhofer ISE had proved it by comparing the cell performance between EWT cells and IBC cells on degraded silicon substrates. An EWT efficiency of 18.7 % on degraded 1.4 Ω cm p-type CZ silicon substrates with bulk lifetime of 35 μs and thickness of 250 μm outperforms clearly the IBC (14.9 %) and even the PERC (18.1 %) cell [243]. The superiority comes mainly from the very high J_{sc} of the EWT cell of more than 41 mA/cm^2 on FZ as well as degraded CZ-Si substrates. This striking difference becomes manifest in very different external and internal quantum efficiencies for EWT and IBC cells, as shown in Fig. 1.20 (reproducible from [243]). From around 400–850 nm, the EQE/IQE of the EWT cell is more than 25 % absolute higher than that of the IBC. This underlines the excellent carrier collection efficiency of the EWT cell compared to the IBC that



Type	Material (p-type)	Voc (mV)	Isc (mA/cm²)	FF (%)	Effic. (%)
EWT	FZ, 1.25 Ω cm	656.1	41.1	75.1	20.2
IBC	FZ, 1.25 Ω cm	665.3	37.1	77.7	19.2
EWT	CZ, 1.4 Ω cm	616.0	40.9	74.1	18.7
IBC	CZ, 1.4 Ω cm	615.5	31.8	76.0	14.9

Fig. 1.20 Measurement of external and internal quantum efficiencies as well as reflection of EWT and IBC cells on degraded 1.4 Ω cm CZ-Si substrates. The *inset table* presents EWT and IBC cell results on 1.25 Ω cm FZ-Si and degraded 1.4 Ω cm CZ-Si substrates. (Reproducible from [243])

cannot cope with medium-quality silicon substrates. As for high-quality Si substrates, a maximum efficiency of 21.4 % on p-type FZ Si substrates with 91.9 cm^2 aperture area has been reported by Engelhart et al. [240, 244] using laser processing and PVD-metallization. The highest efficiency on industrial p-type monocrystalline material quality (1.4 Ω cm CZ-Si) is 20.3 % achieved by Lim et al. using laser-processing and PVD-metallization with a comparatively simple process ("RISE-EWT") [245]. The abbreviation "RISE" means a Rear side Interdigitated contact pattern and mask-free metallization by a Single vacuum Evaporation step. This process involves only one phosphorus diffusion and one thermal oxidation process step and thus is considered suitable for large-scale industrial production. In a recent study published by Mingirulli et al. [246], designated area (16.7 cm^2) conversion efficiencies of up to 18.8 % on FZ materials have been obtained by applying the single step side SE fabrication unique and conventional screen-printing for metallization instead of PVD-metallization. Apart from the mainstream studies on p-type Si EWT cells, Kiefer et al. [247] from the Institute for Solar Energy Research Hamelin (ISFH), Germany, have developed high-efficiency EWT cells for n-type silicon wafers. By passivating the front and rear boron-diffused p-type emitter by a stack of aluminium oxide and silicon nitride (Al_2O_3-SiN_x) and using a $POCl_3$-diffusion process that forms a BSF as shown in Fig. 1.18, they have demonstrated a record efficiency of 21.6 % (V_{oc} = 661 mV, J_{sc} = 40.4 mA/cm^2, FF = 80.8 %) on small area (4 cm^2) 1.5 Ω cm CZ-Si substrates [247].

Despite these high performances, EWT cells have not yet performed as well as expected, because their efficiency levels are usually reduced by small fill factors (FFs) [237, 239, 240, 243, 244]. Recently, Ulzhöfer et al. [238, 248] have demonstrated that a recombination enhancement caused by lateral current flows is

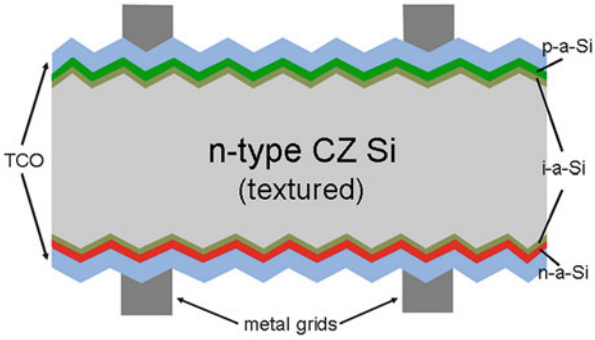


Fig. 1.21 The schematic structure of the n-type CZ-Si HIT cell developed by Sanyo

responsible for reducing the FF and efficiency, particularly for relatively high wafer resistivities higher than 3 Ω cm. It is shown [238] that the critical parameter for optimizing FF is the base resistivity, which strongly determines the injection-dependent excess carrier density and the recombination mechanisms in the base. For this reason, silicon wafers with low resistivities are often used as silicon substrates for high-efficiency EWT cells.

3.6 HIT Solar Cells

Heterojunction with intrinsic thin-layer (HIT) solar cell is an improved version of silicon heterojunction (SHJ) solar cell, which was first proposed by Fuhs et al. [249]. SHJ solar cells composed of a-Si/c-Si use only doped hydrogenated amorphous silicon (p-type or n-type a-Si:H) as the emitter and contact layers on c-Si substrates, so the resultant efficiencies are usually low due to the unpassivated c-Si surfaces. In order to achieve high-efficiency devices, Sanyo Co. Ltd [250, 251] developed a new a-Si/c-Si heterojunction structure called HIT, which features a very thin intrinsic a-Si layer inserted between the doped a-Si layer and the c-Si substrate. This simple yet novel structure has been attracting a growing amount of attention year by year. This is because: (1) it simultaneously enables an excellent surface passivation and p–n junction, resulting in high efficiency; (2) its low-temperature processes (<200 °C) can prevent any degradation of bulk quality that happen with high-temperature cycling processes in low-quality silicon materials such as solar grade CZ Si; and (3) compared with conventional diffused cells, a much better temperature coefficient can be obtained with high-V_{oc} cells [38, 40, 252] (Fig. 1.21).

A typical scheme of the n-type Si HIT solar cell developed by Sanyo is shown in Fig. 1.22. The n-type 250-μm-thick CZ Si substrate is first cleaned and textured for double sides. The p–n junction is usually created by the deposition of intrinsic a-Si and p-type a-Si layers on the n-type textured c-Si substrate with the PECVD method. On the rear side, the BSF structure is achieved by depositing intrinsic

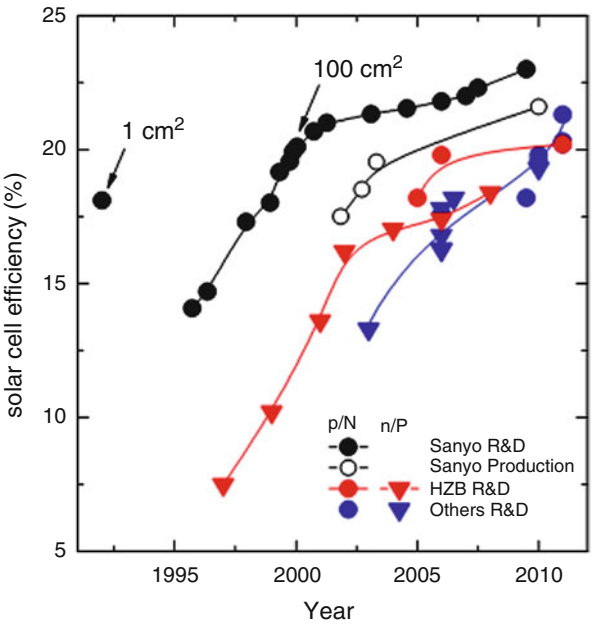


Fig. 1.22 Conversion efficiencies development of HIT solar cells in Sanyo, Helmholtz Zentrum Berlin (HZB) and other research institutes. HZB group achieved maximum efficiencies of 19.8 % and 17.8 % on n-type and p-type c-Si, respectively. (Reproducible from [257])

a-Si and n-type a-Si layer stacks. On both deposited surfaces, TCO layers and metal electrodes are formed with the sputtering and screen-printing method, respectively. All processes (including metallization process) are performed at temperatures of below 200 °C. As Sect. 2.4 describes, the TCO layer on the front surface also works as a transparent and anti-reflection (AR) layer through the optimization of its thickness. In general, the finger electrode on the AR layer is narrower than that of conventional p–n diffused solar cells, to compensate for the poor sheet resistance of the TCO layer. As for the electrode on the back, the researchers in Sanyo Co. Ltd [38, 40, 252] also use a finger electrode to make the HIT cell symmetrical between front and rear so that the thermal and mechanical stresses in the device can be reduced. Therefore, this solar cell is suitable for various applications, such as the bifacial modules. This symmetrical structure and the low temperature processes further offer the advantage of decreasing the thickness of the cell and reducing the production cost.

The most striking feature of the HIT cell is the very high efficiency (>20 %) realized with a simple fabrication process. This high efficiency is highly associated with the high open-circuit voltage (V_{oc}) (>700 mV) due to the effective carrier trapping within the generation region (c-Si) of the symmetrical heterostructure. In comparison, for a simple p-a-Si/n-c-Si SHJ structure, only a V_{oc} of less than 600 mV can be obtained [40]. In the p/n heterojunction, the interface state density caused by the doping materials, which attach to the c-Si surface during the deposition process, seems to deteriorate the junction properties significantly. By inserting an intrinsic layer into the p-a-Si/n-c-Si heterojunction, these defects caused by the doping materials can be avoided and thus the junction properties could be improved

drastically [253]. Furthermore, as Sect. 2.3.5 discusses, the intrinsic a-Si:H layer can play as an excellent passivation scheme on c-Si wafers and help reduce the recombination at the heterointerface.

The evolution of HIT cell efficiency can be traced back to 1994, when an efficiency of 20 % has been achieved for an aperture area of 1 cm^2 by Sanyo [251]. After that, Sanyo devoted to creating a better heterointerface by cleaning the c-Si wafer as much as possible and using a low-damage plasma deposition processes for high-quality a-Si:H films [38, 40, 252]. Therefore, in 2004, an even higher conversion efficiency of 21.5 % (V_{oc} = 712 mV, I_{sc} = 3.837 A, FF = 78.7 %) with a size of 100.3 cm^2 has been achieved in their laboratory [40]. By further optimizing the viscosity and rheology of the silver paste and the process parameters in the screen printing, the grid electrode with lower resistance and finer lines (without a spreading area) can be achieved. Therefore, the cell efficiency can be further enhanced by about 1.6 % [150]. By developing high-quality wide-gap alloys such as a-SiC:H and high-quality TCO with high carrier mobility, the optical losses can be further reduced and thus a higher I_{sc} can be obtained [150]. As a result of these progressive studies, Sanyo have achieved a higher efficiency of 22.3 % (V_{oc} = 725 mV, I_{sc} = 3.909 A, FF = 79.1 %) with a total size of 100.5 cm^2 in 2007 [150, 254]. Later in 2009, the conversion efficiency of the standard HIT solar cell developed by Sanyo has reached a record level of 23.0 % for a 100.4 cm^2 practical size n-type c-Si substrate (V_{oc} = 729 mV, J_{sc} = 39.52 mA/cm^2, FF = 80.0 %) [255]. Furthermore, Sanyo has customized these high-efficiency technologies to develop thinner-substrate (98 μm) HIT solar cells. By developing new technologies consisting of a new device design, an improved junction formation process and an enhanced optical confinement, they have obtained a conversion efficiency of 22.8 % (V_{oc} = 743 mV, J_{sc} = 38.84 mA/cm^2, FF = 79.1 %) for a 98-μm-thick practical size cell [255, 256]. Figure 1.22 presents the history of conversion efficiency for HIT solar cells developed by Sanyo both in R&D and mass production (reproducible from [257]). During the last few years, they have accelerated the improvement of the conversion efficiency. Surprisingly, the efficiency of 22.8 % for thinner-substrate (98 μm) is comparable to the best efficiency of 23.0 % for standard substrate (250 μm). Reducing the thickness of the substrates by more than 50 % and maintaining its efficiency at the same time provides the possibility of further reducing the cost production of HIT solar cells.

While Sanyo has focused on n-type CZ-Si substrates, European and US groups have concentrated on developing the HIT solar cell on both n-type and p-type Si substrates [258–263], as summarized in Fig. 1.22. In 2010, Roth and Rau obtained a conversion efficiency of 21.0 % [258] on 4 cm^2 area and 19.3 % [259] on 148 cm^2 area for FZ n-type Si substrates with a resistivity of 3 Ω cm. At Institute of Microengineering (IMT) in Neuchâtel, Switzerland, Descoeudres et al. [260] have achieved a conversion efficiency of 20.3 % on 4 cm^2 area for 300-μm-thick 4 Ω cm FZ n-type Si substrates, and then improved the efficiency to 21.0 % [261] by using H_2 plasma treatment to enhance the surface passivation. In contrast, p-type Si HIT solar cells usually exhibit inferior performances as compared with those HIT

cells fabricated on n-type Si substrates. For example, Wang et al. [262] at National Renewable Energy Laboratory (NERL) have achieved remarkable efficiencies of 19.3 % (V_{oc} = 678 mV, J_{sc} = 36.20 mA/cm^2, FF = 78.61 %, area = 0.9 cm^2) and 18.8 % (V_{oc} = 670.1 mV, J_{sc} = 36.71 mA/cm^2, FF = 76.56 %, area = 0.81 cm^2) on 220–330-μm-thick 1–4 Ω cm p-type FZ-Si and CZ-Si textured substrates, respectively, while Damon-Lacoste et al. [263] at LPICM-Ecole Polytechnique Paris have achieved a low efficiency of 17.1 % (V_{oc} = 664 mV, J_{sc} = 33 mA/cm^2, FF = 77.8 %, area = 0.81 cm^2) on 330-μm-thick 1–4 Ω cm p-type CZ-Si flat substrates. The lower efficiency may be attributed to the lower J_{sc} value obtained with non-textured wafers. The roadmap of the conversion efficiency of the HIT solar cells based on p-type Si substrates has also been summarized in Fig. 1.22. It is obvious that the inferior cell performance of HIT solar cells fabricated on p-type substrates is highly related to the lower value of V_{oc} as compared to the corresponding HIT solar cells fabricated on n-type substrates. In particular, for n-type HIT solar cells developed by Sanyo, the maximum V_{oc} can easily exceed 700 mV, whereas that for p-type HIT solar cells is usually in a range between 660 and 690 mV.

In order to explain the different cell performance between n-type HIT solar cells and p-type HIT solar cells, the band diagrams of n-type and p-type bifacial heterojunction devices are depicted in Fig. 1.23a, b, respectively. In the case of n-type wafers (a), the minority carriers of hole are collected in the front side electrode, and the majority carrier of electrons are collected in the back side electrode. The large valence band offset at the front junction results in such a potential well where hole could be trapped, preventing efficient photogenerated carrier transport. However, the trapped carrier holes may be able to pass through the thin (i)a-Si:H layer into the (p)a-Si:H emitter by the aid of the tunneling and hopping. On the back side, the large valence band offset provides a field effect passivation as demonstrated in Sect. 2.3.1, minimizing the surface recombination on the back side. The small conduction band offset allows efficient electron collection at the back side contact. Thus the (i/n)a-Si:H stack at the back side provides an excellent back contact with adequate majority carrier electron transport and excellent passivation repelling minority carrier holes from the back contact. In such case, an extraordinarily high open-circuit voltage of >700 mV can be achieved for n-type HIT solar cells.

By contrast, in the case of p-type wafers as shown in Fig. 1.23b, the minority carrier electrons are collected on the front side electrodes, and the majority carrier holes are collected on the back side electrode. The minority transport is easier than in N-type c-Si case because of the smaller band offset in the entire path. However, lower open-circuit voltages are expected since the built-in potential (from the vacuum level bending) at the front junction is comparable to a homojunction, much less than that on n-type wafers. On the back side, the small conduction offset provides a much less effective mirror for the minority carrier electrons. Worse, the larger offset in the valence band edges would present a large barrier for majority

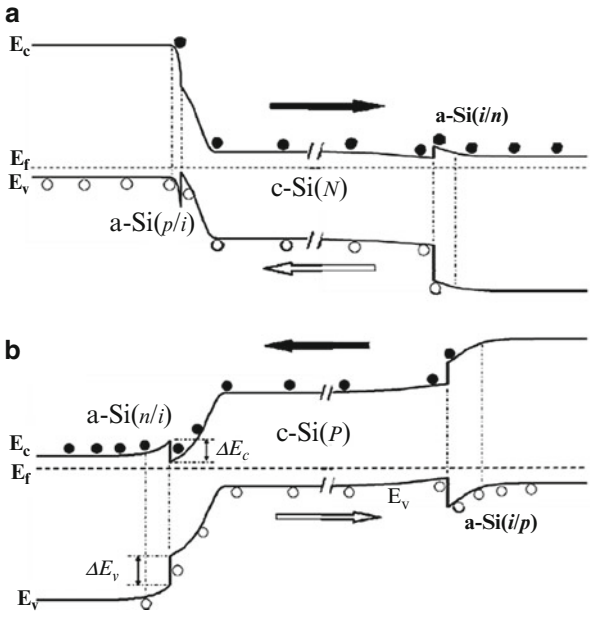


Fig. 1.23 The band diagrams of the bifacial junction HIT solar cells based on the n-type (**a**) and p-type (**b**) c-Si wafers. The transport direction of the hole (*open circles*) and electron (*solid circles*) is schematically marked by the *hollow* and *solid arrows*, respectively

carrier holes to be collected at the back side contact. Though thinner or i-layer suppression can favour tunneling transport, the passivation quality would be partially reduced in such case. Therefore, the open-circuit voltage cannot exceed 700 mV for p-type HIT solar cells and thus the efficiency is limited to below 20 % consequently.

Since the fabrication of HIT solar cells involves a large number of processing variables, such as the doping concentration of the amorphous emitter, the thickness of the intrinsic and doped a-Si:H layer, the deposition of TCO films and metal electrodes, the band alignment of a-Si/c-Si heterojunction, etc., it is a formidable task to scrutinize the effect of each variable on the cell performance experimentally. Numerical simulation using AMPS or AFORS-HET software is often adopted as a convenient way to accurately evaluate the role of various parameters [264–268]. In a recent simulation [267], modeling indicates that the defect on the front surface of c-Si reduce the open-circuit voltage and fill factor, while those on the rear surface degrade mainly the short-circuit current density and fill factor. It has also been found by simulation [268] that not only the transparency and conductivity but also the work function of TCO films can affect the cell performance obviously.

4 Summary

The interest and quest for high-efficiency Si solar cells has attracted more and more attention from researchers, scientists and engineers in both academia and industry for the past several decades. Of all the materials that are discussed in this review, Si material is the core material for Si solar cells while passivation material is the critical material for high-efficiency Si solar cells. Thermally grown SiO_2 has seldom been adopted as the passivation scheme for high-efficiency Si solar cells in recent years since its deposition processes are not desirable from not only the throughput but also the process compatibility viewpoint due to extremely high-temperature process and low deposition rate. In comparison, a-Si:H, SiO_x, SiN_x and Al_2O_3 layers deposited by plasma processes as well as their layer stacks such as SiO_x/SiN_x, Al_2O_3/SiN_x and a-Si:H/SiN_x have been given a lot of importance owning to their excellent passivation qualities and relatively easier deposition conditions, particularly in the fabrication of high-efficiency PERC, PERL, IBC, EWT and HIT solar cells. Among all the high-efficiency devices that are reviewed in this chapter, PERC, PERL and HIT solar cells are most promising for mass production in industrial scale due to the minimization of the use of high-temperature processes and photolithography techniques. Indeed, Pluto-PERC and Pluto-PERL cells as well as HIT cells have been produced in elementary industrial scale by Suntech and Sanyo, respectively. Applying these delicate and advanced cell designs and concepts to industrial Si wafer-based solar cells without increasing production cost still remains a challenge and needs further research.

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